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Liu et al.

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(45) **Date of Patent: Oct. 18, 2016**

(54) **RESISTIVE MEMORY ARCHITECTURES WITH MULTIPLE MEMORY CELLS PER ACCESS DEVICE**

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(73) Assignee: **OVONYX MEMORY TECHNOLOGY, LLC**, Alexandria, VA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/617,377**

(22) Filed: **Feb. 9, 2015**

(65) **Prior Publication Data**

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Related U.S. Application Data

(60) Division of application No. 13/292,884, filed on Nov. 9, 2011, now Pat. No. 8,976,562, which is a continuation of application No. 12/656,720, filed on Feb. 16, 2010, now Pat. No. 8,076,195, which is a division of application No. 11/806,495, filed on May 31, 2007, now Pat. No. 7,684,227.

(51) **Int. Cl.**

H01L 45/00	(2006.01)
H01L 27/24	(2006.01)
G11C 13/00	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 45/1253*** (2013.01); ***G11C 13/003*** (2013.01); ***G11C 13/0004*** (2013.01); ***G11C 13/0023*** (2013.01); ***G11C 13/0026*** (2013.01); ***H01L 27/2409*** (2013.01); ***H01L 27/2436*** (2013.01); ***H01L 27/2472*** (2013.01);

(Continued)

(58) **Field of Classification Search**

CPC H01L 45/06; H01L 45/1253; H01L 27/2409; H01L 27/2436; G11C 13/0004; G11C 13/003

See application file for complete search history.

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Primary Examiner — Allison P Bernstein

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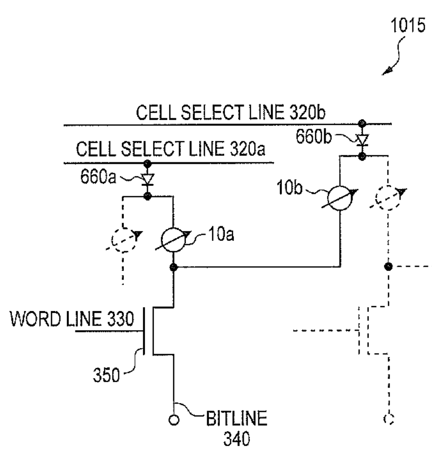
(57) **ABSTRACT**

A resistive memory structure, for example, phase change memory structure, includes one access device and two or more resistive memory cells. Each memory cell is coupled to a rectifying device to prevent parallel leak current from flowing through non-selected memory cells. In an array of resistive memory bit structures, resistive memory cells from different memory bit structures are stacked and share rectifying devices.

15 Claims, 43 Drawing Sheets



(52) **U.S. Cl.**
CPC ***H01L27/2481*** (2013.01); ***H01L 45/06*** (2013.01); ***H01L 45/1233*** (2013.01); ***H01L 45/144*** (2013.01); *G11C 2213/72* (2013.01); *G11C 2213/74* (2013.01); *G11C 2213/76* (2013.01); *G11C 2213/78* (2013.01); *G11C 2213/79* (2013.01)

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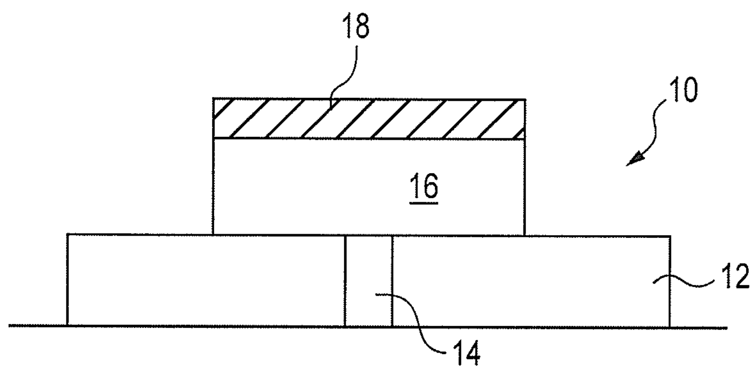


FIG. 1
(PRIOR ART)

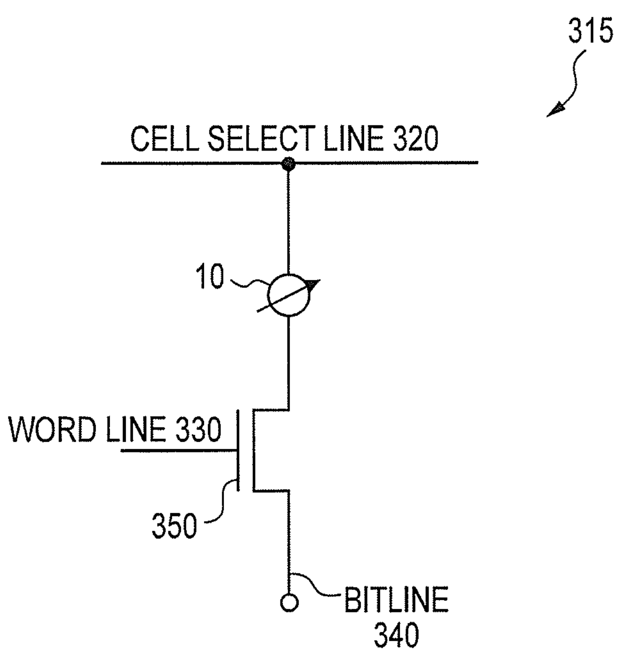


FIG. 2A
(PRIOR ART)

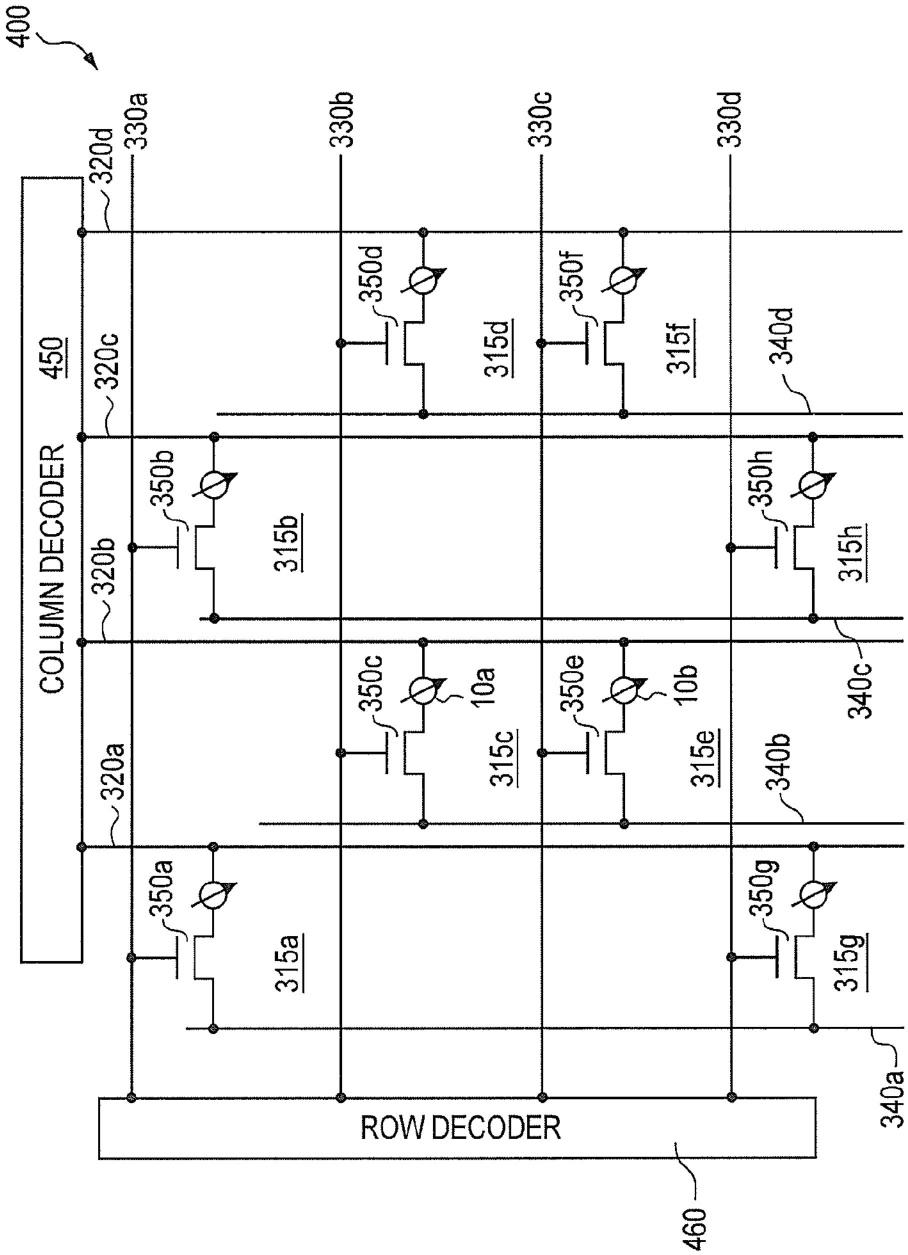


FIG. 2B
(PRIOR ART)

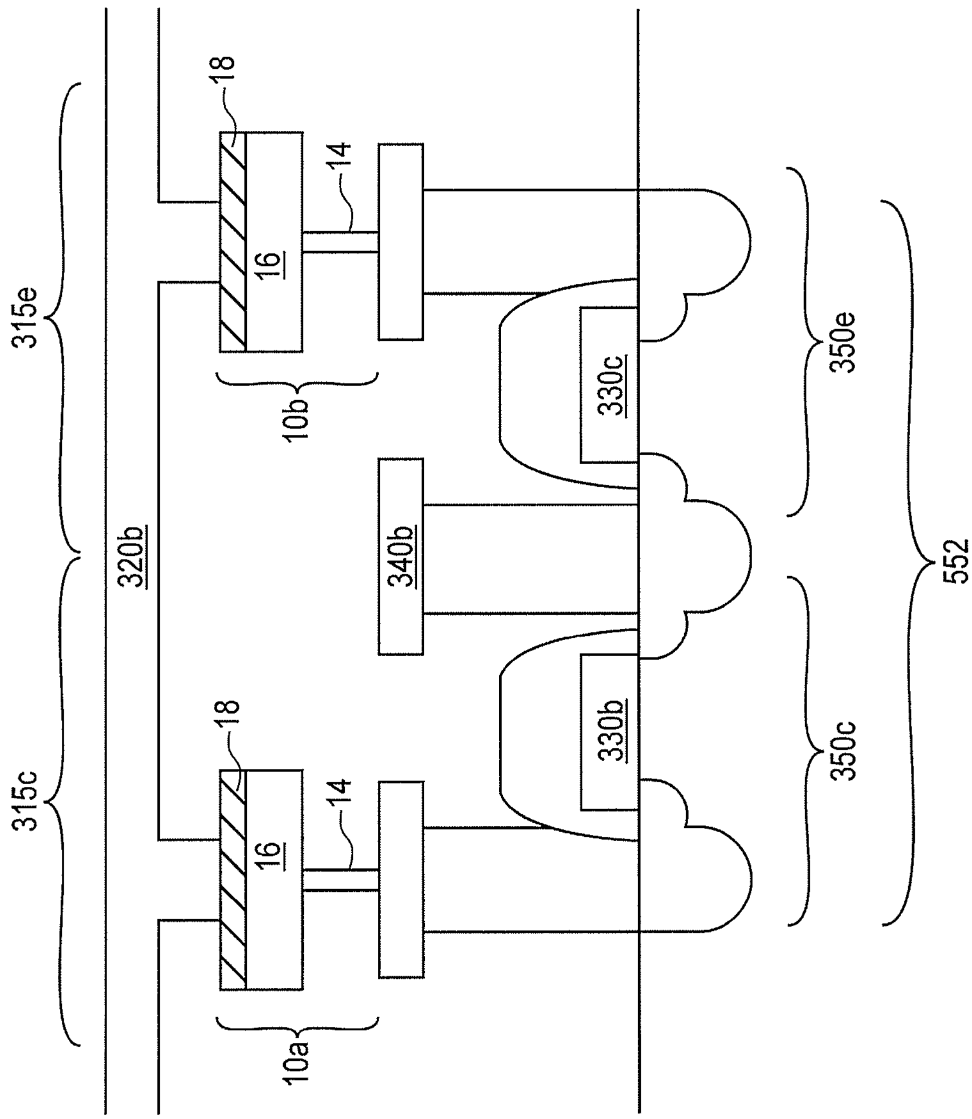

315e
315c
320b
18
14
16
10b
18
14
16
10a
340b
330c
330b
350e
350c
552

FIG. 2C

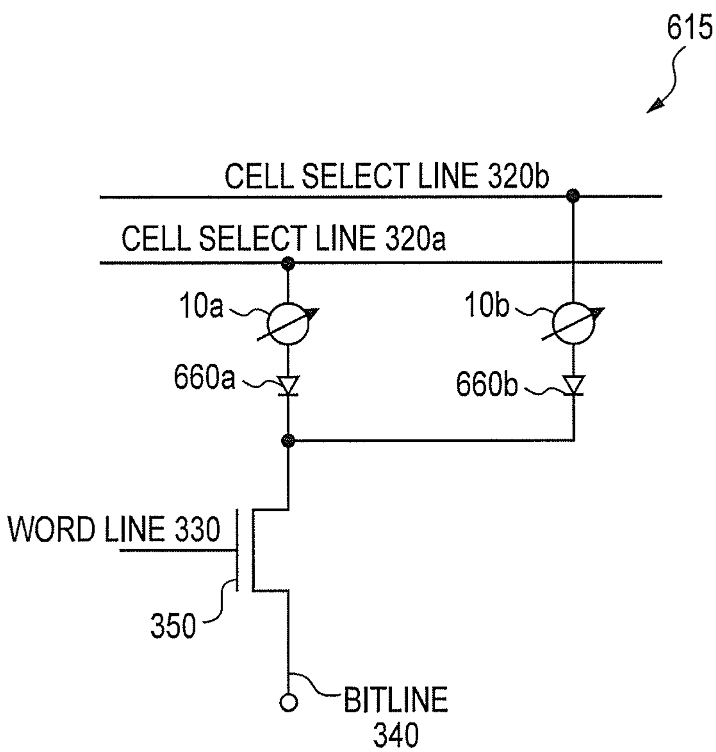

615
CELL SELECT LINE 320b
CELL SELECT LINE 320a
10a
10b
660a
660b
WORD LINE 330
350
BITLINE
340

FIG. 3

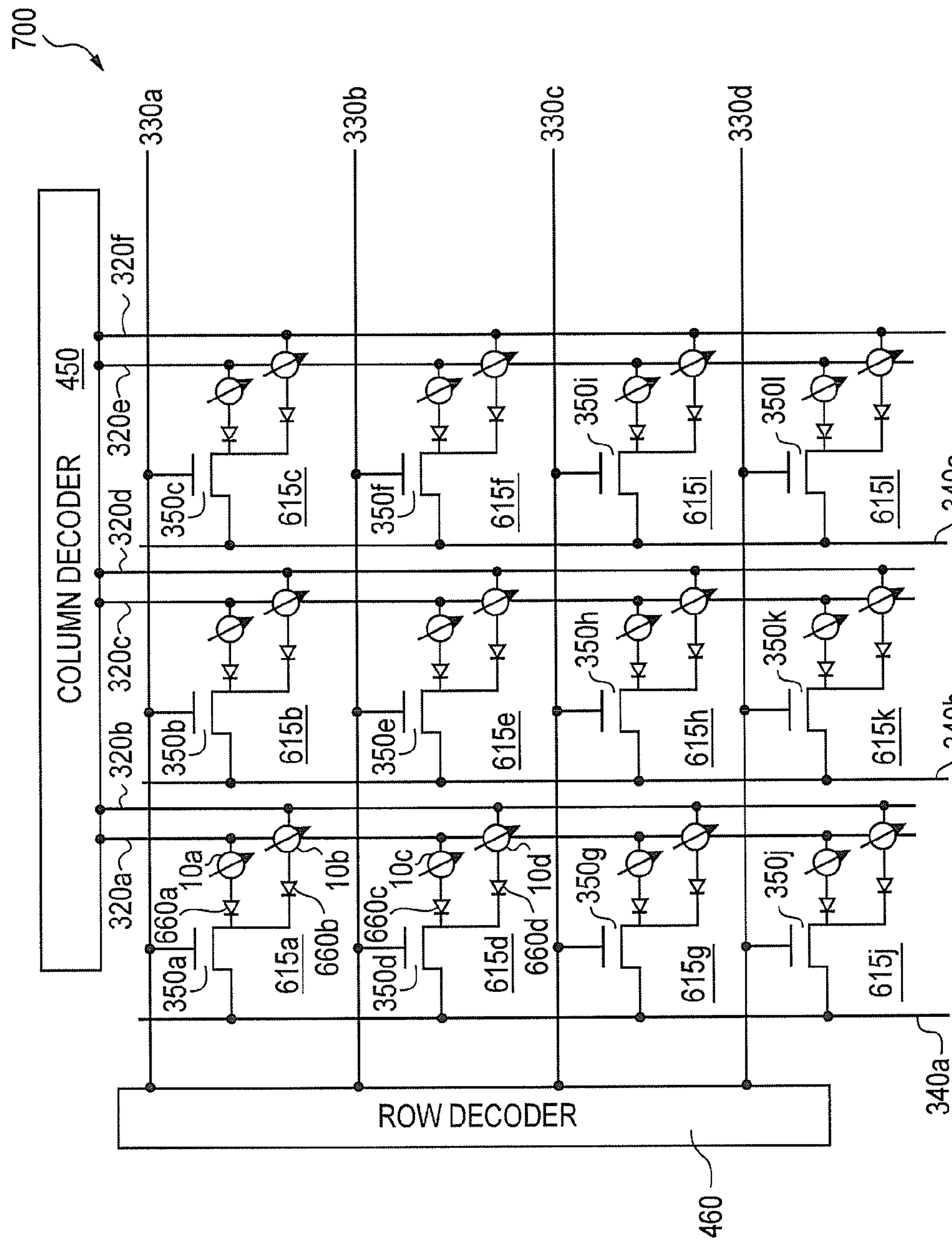

700
330a
330b
330c
330d
COLUMN DECODER
450
320a
320b
320c
320d
320e
320f
340a
340b
340c
350a
350b
350c
350d
350e
350f
350g
350h
350i
350j
350k
350l
615a
615b
615c
615d
615e
615f
615g
615h
615i
615j
615k
615l
660a
660b
660c
660d
10a
10b
10c
10d
ROW DECODER
460

FIG. 4A

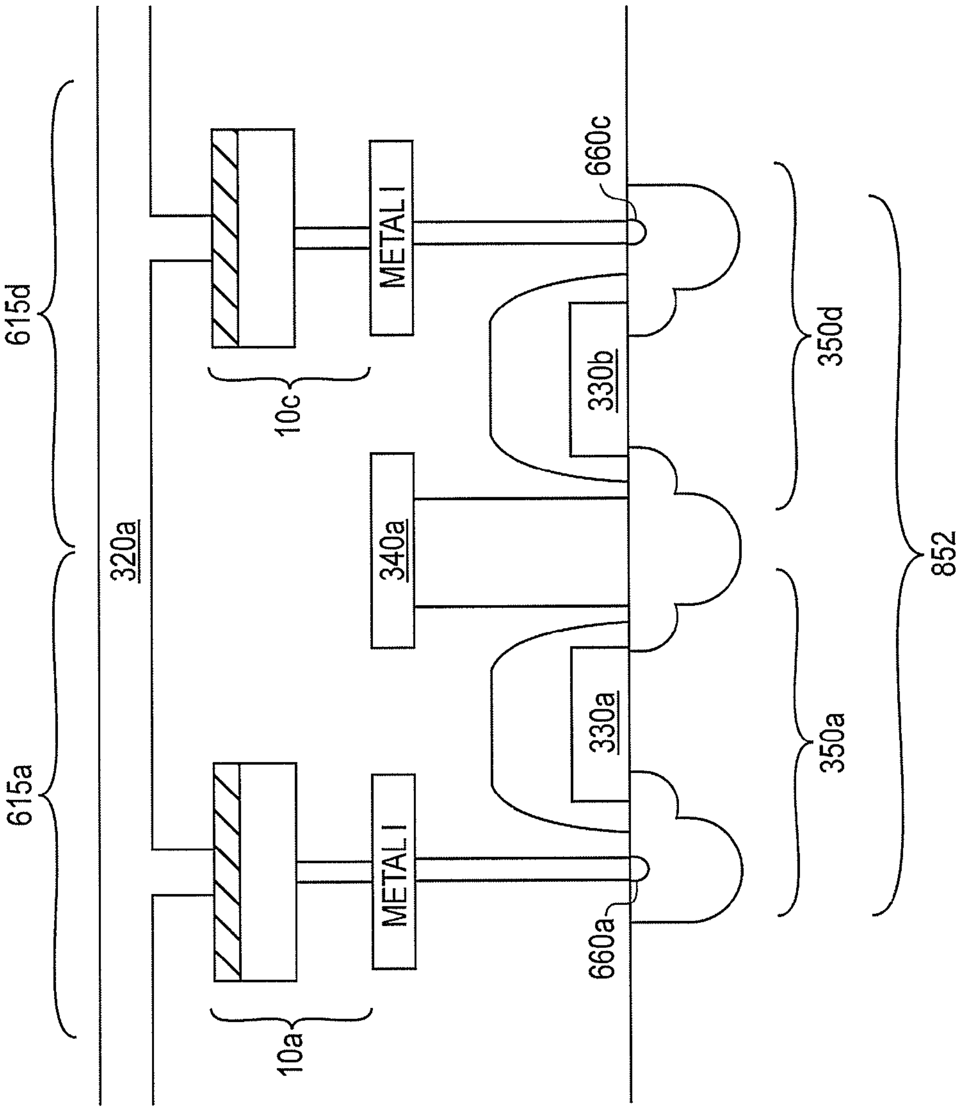

615d
615a
320a
10c
10a
METAL I
METAL I
340a
330b
330a
660c
660a
350d
350a
852

FIG. 4B

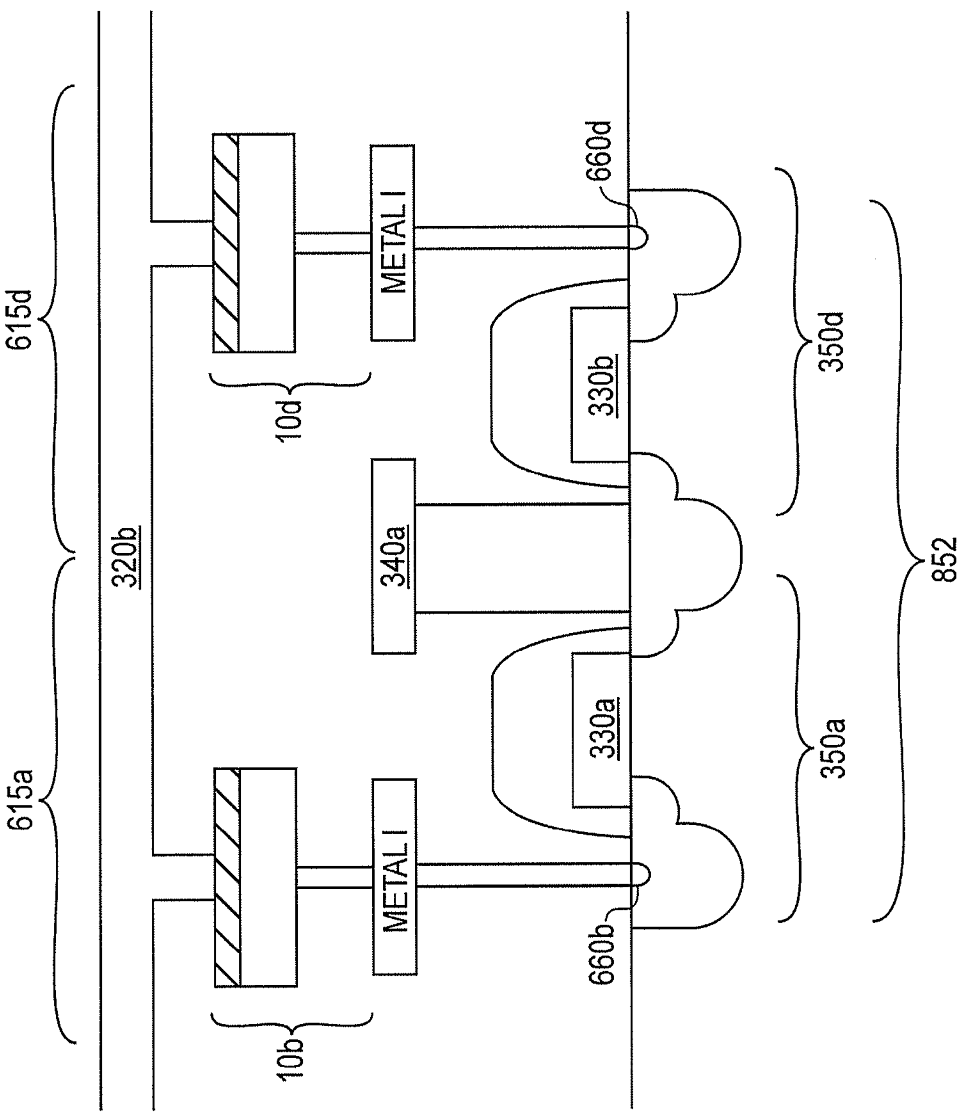

615d
615a
320b
10d
10b
METAL I
METAL I
340a
330b
330a
660d
660b
350d
350a
852

FIG. 4C

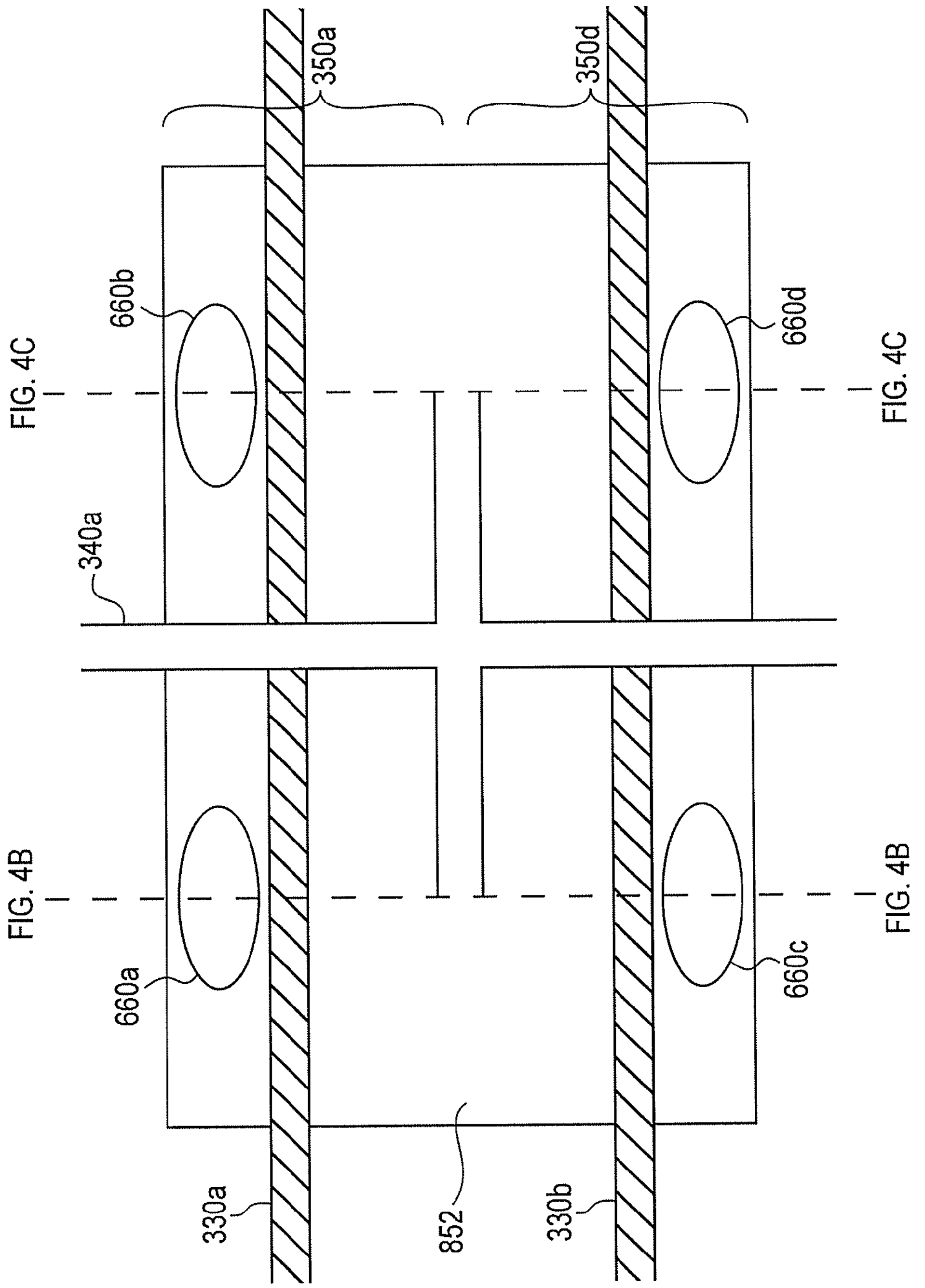

350a
350d
660b
660d
FIG. 4C
FIG. 4C
340a
FIG. 4B
FIG. 4B
660a
660c
330a
852
330b

FIG. 4D

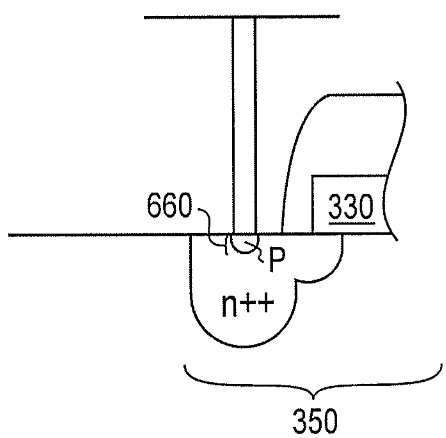
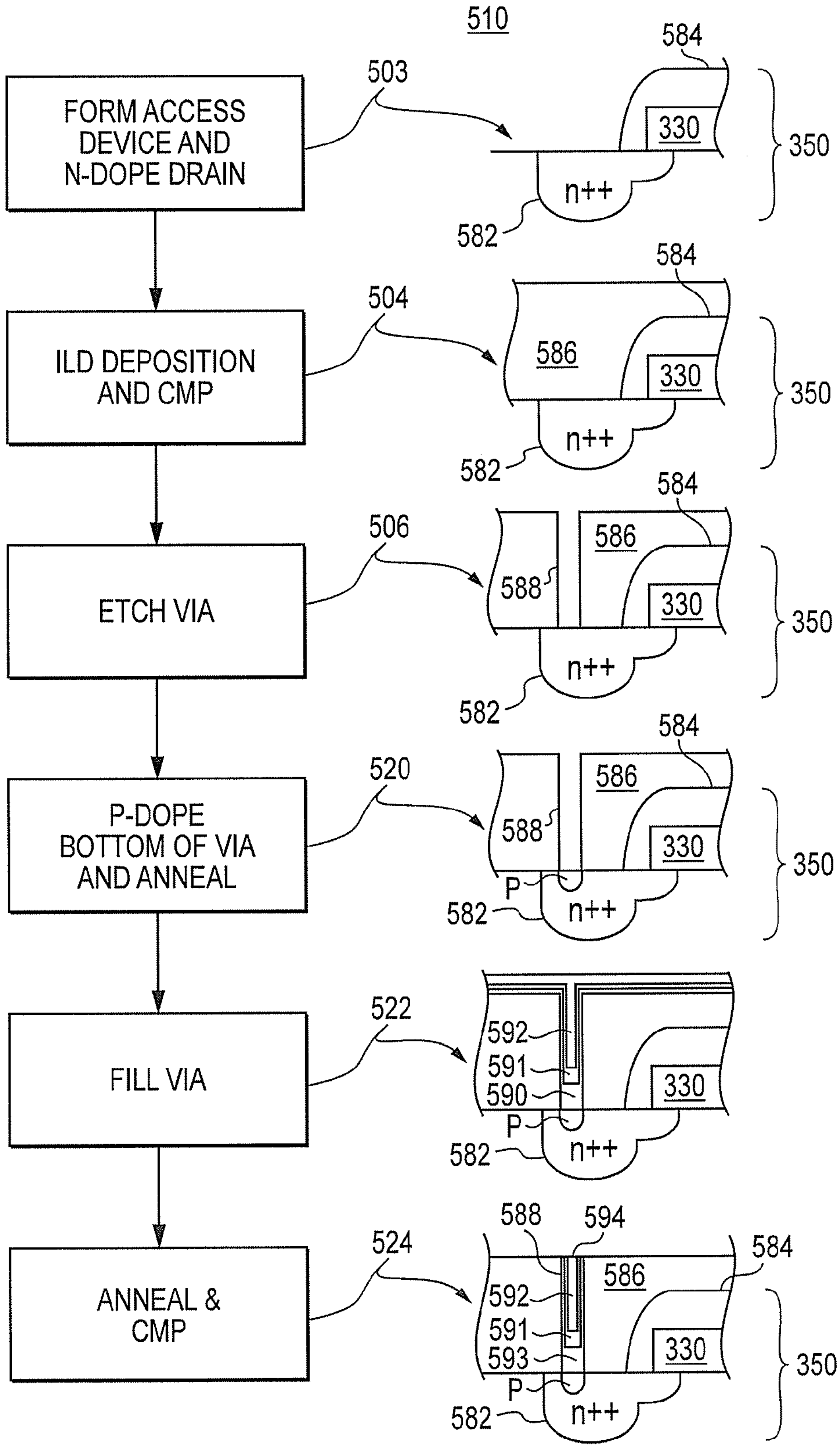


FIG. 5A



510
FORM ACCESS DEVICE AND N-DOPE DRAIN
503
584
330
n++
582
350
ILD DEPOSITION AND CMP
504
586
ETCH VIA
506
588
P-DOPE BOTTOM OF VIA AND ANNEAL
520
P
FILL VIA
522
592
591
590
ANNEAL & CMP
524
594
593

FIG. 5B

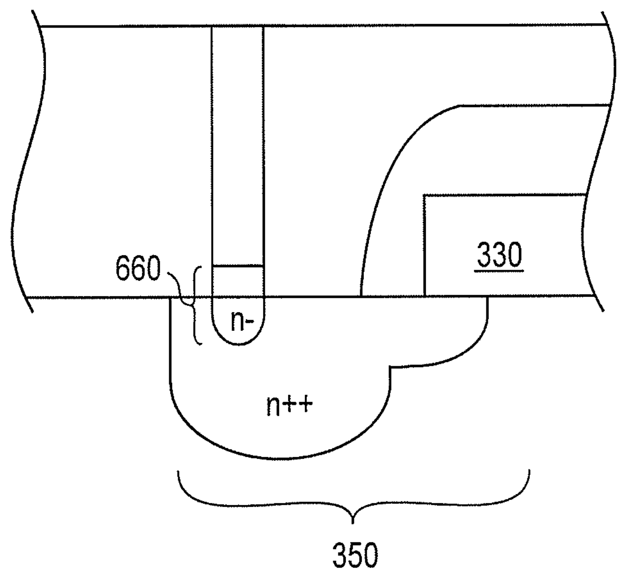


FIG. 5C

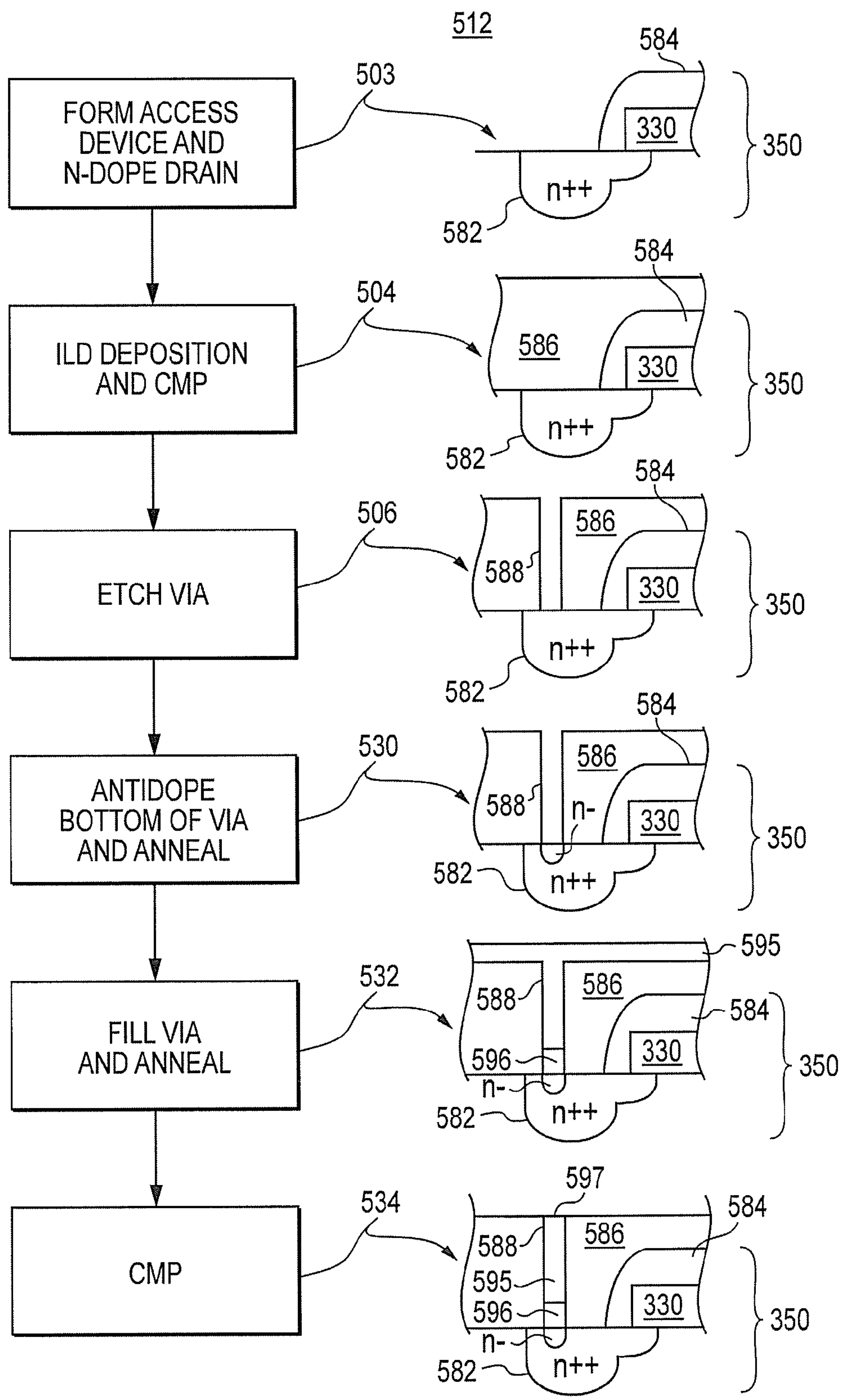

512
FORM ACCESS DEVICE AND N-DOPE DRAIN
503
584
330
350
n++
582
ILD DEPOSITION AND CMP
504
586
ETCH VIA
506
588
ANTIDOPE BOTTOM OF VIA AND ANNEAL
530
n-
FILL VIA AND ANNEAL
532
595
596
CMP
534
597

FIG. 5D

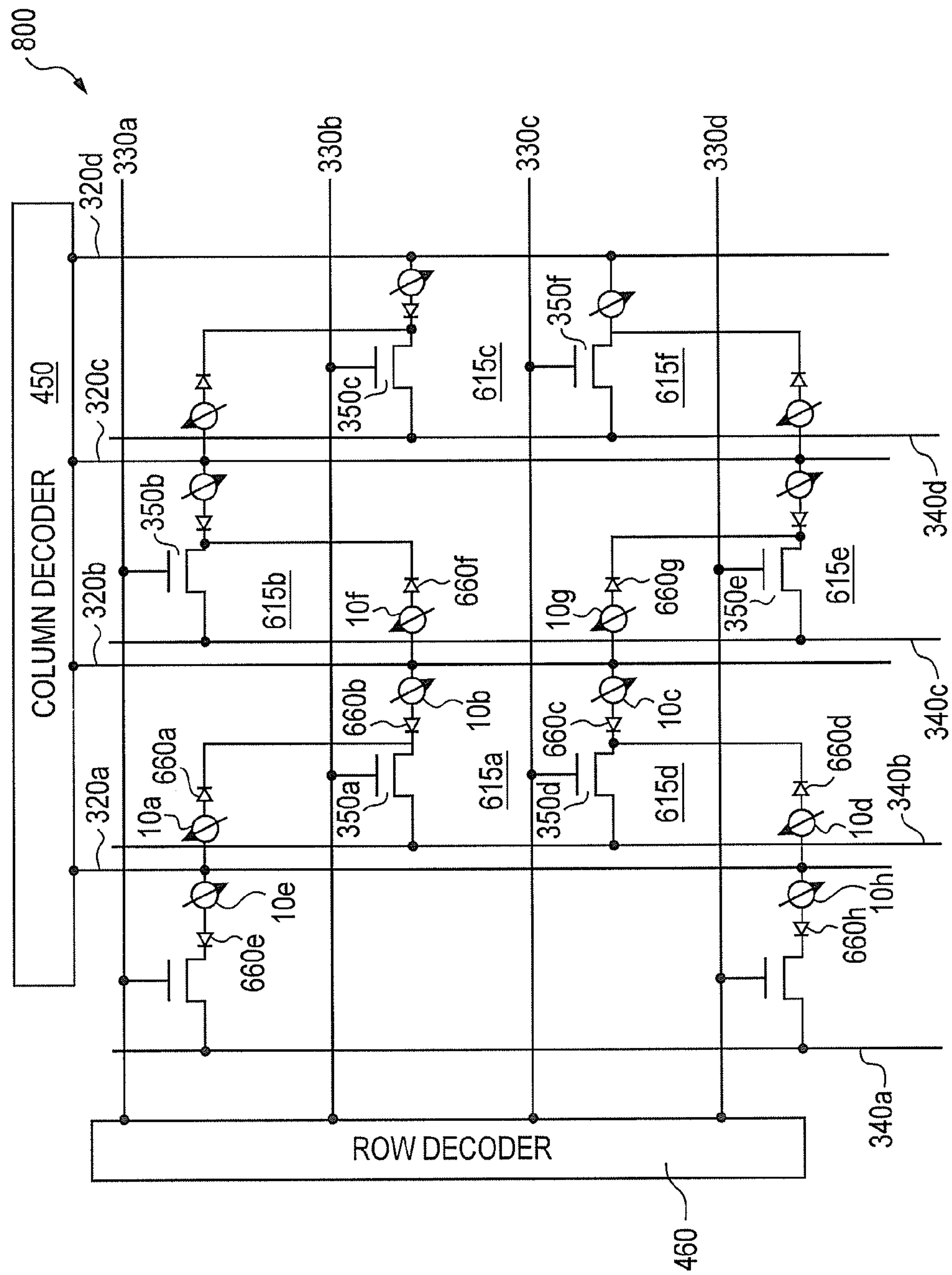

800
COLUMN DECODER
450
ROW DECODER
460
320a
320b
320c
320d
330a
330b
330c
330d
340a
340b
340c
340d
350a
350b
350c
350d
350e
350f
615a
615b
615c
615d
615e
615f
660a
660b
660c
660d
660e
660f
660g
660h
10a
10b
10c
10d
10e
10f
10g
10h

FIG. 6A

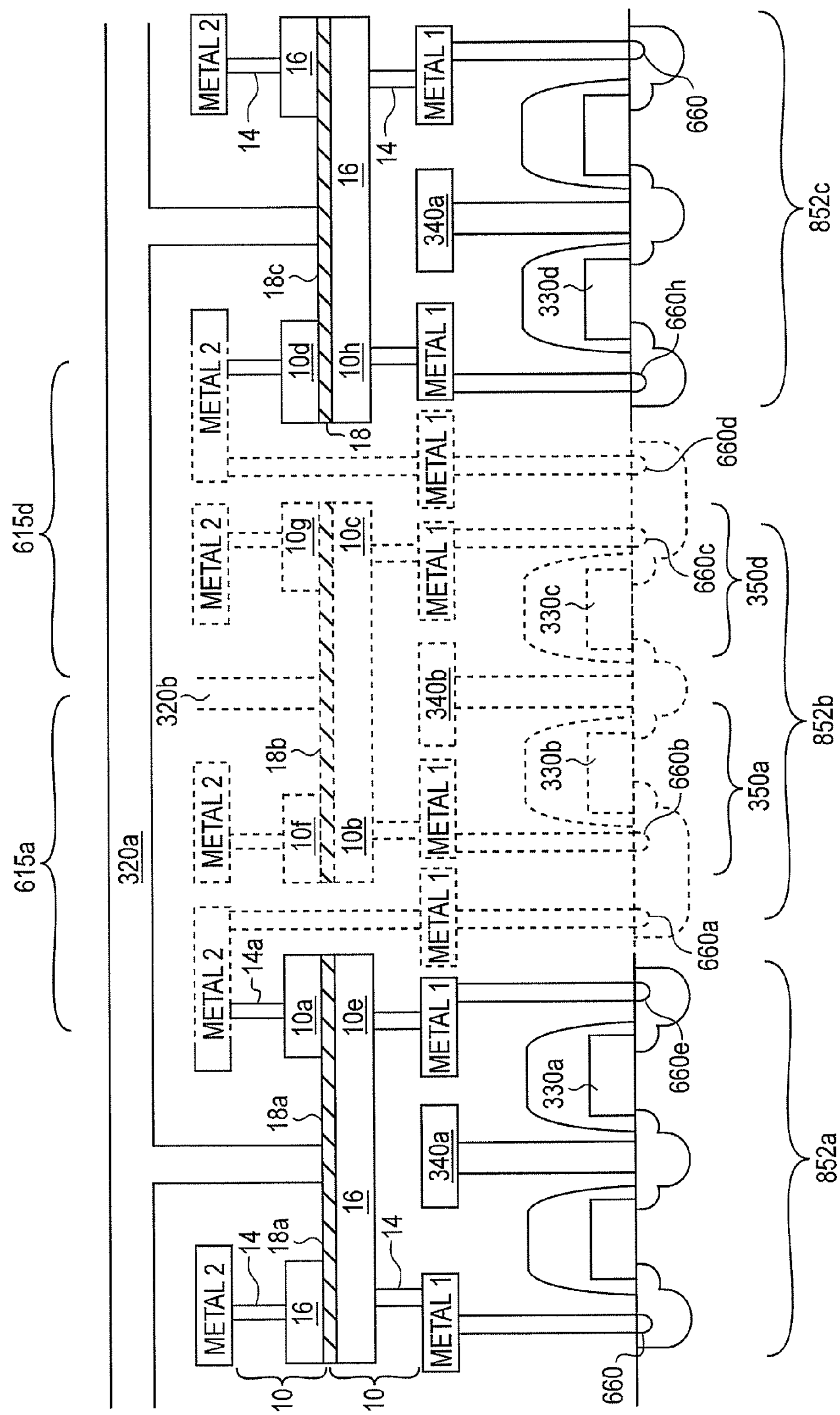

615a
615d
320a
320b
METAL 2
METAL 1
10
10a
10b
10c
10d
10e
10f
10g
10h
14
14a
16
18
18a
18b
18c
330a
330b
330c
330d
340a
340b
350a
350d
660
660a
660b
660c
660d
660e
660h
852a
852b
852c

FIG. 6B

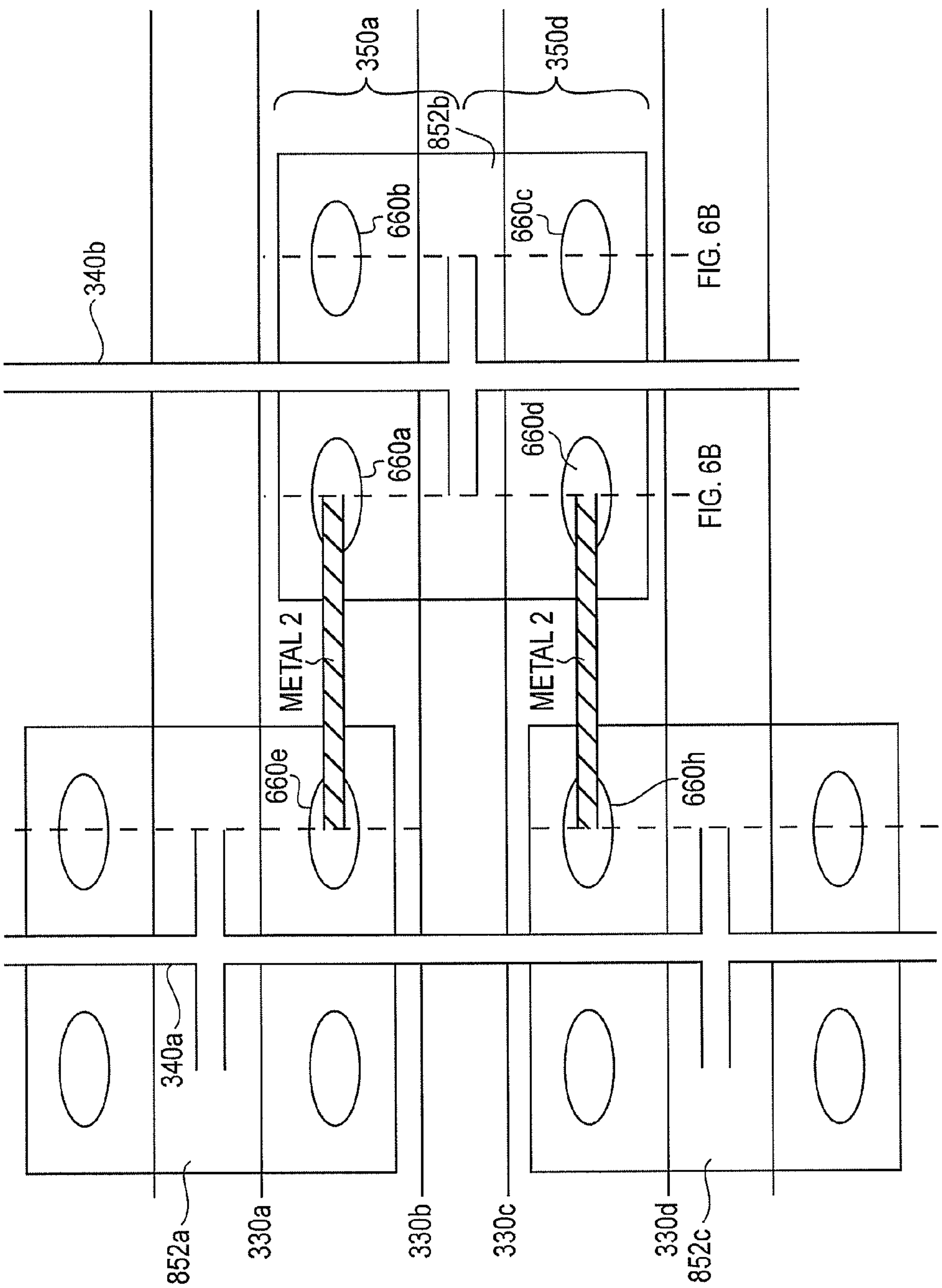

340b
350a
350d
852b
660b
660c
FIG. 6B
660a
660d
FIG. 6B
METAL 2
METAL 2
660e
660h
FIG. 6B
340a
852a
330a
330b
330c
330d
852c

FIG. 6C

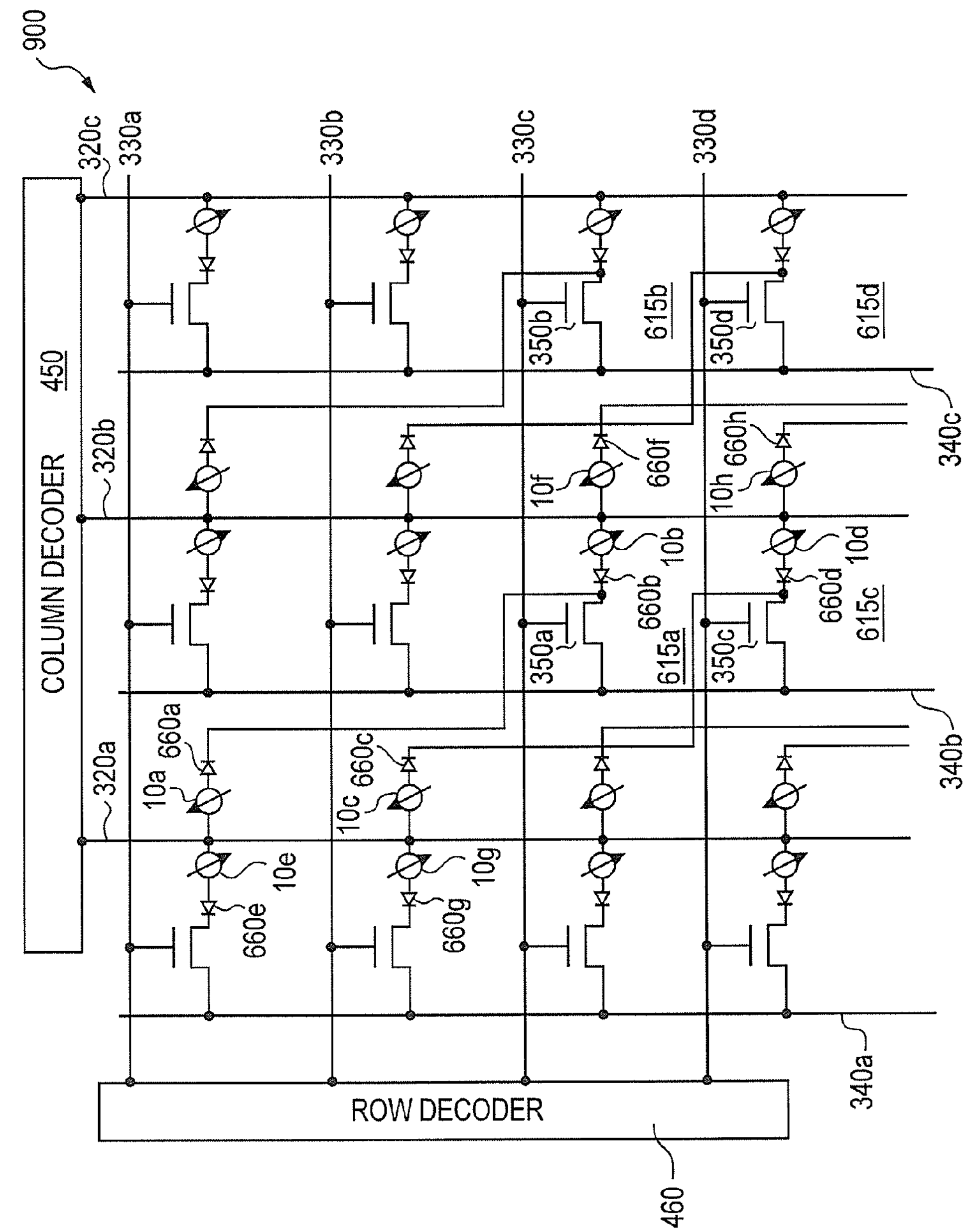

900
320c
330a
330b
330c
330d
COLUMN DECODER
450
320b
320a
350b
615b
350d
615d
340c
10a
660a
10c
660c
10f
660f
10h
660h
10b
660b
10d
660d
350a
615a
350c
615c
340b
10e
660e
10g
660g
340a
ROW DECODER
460

FIG. 7A

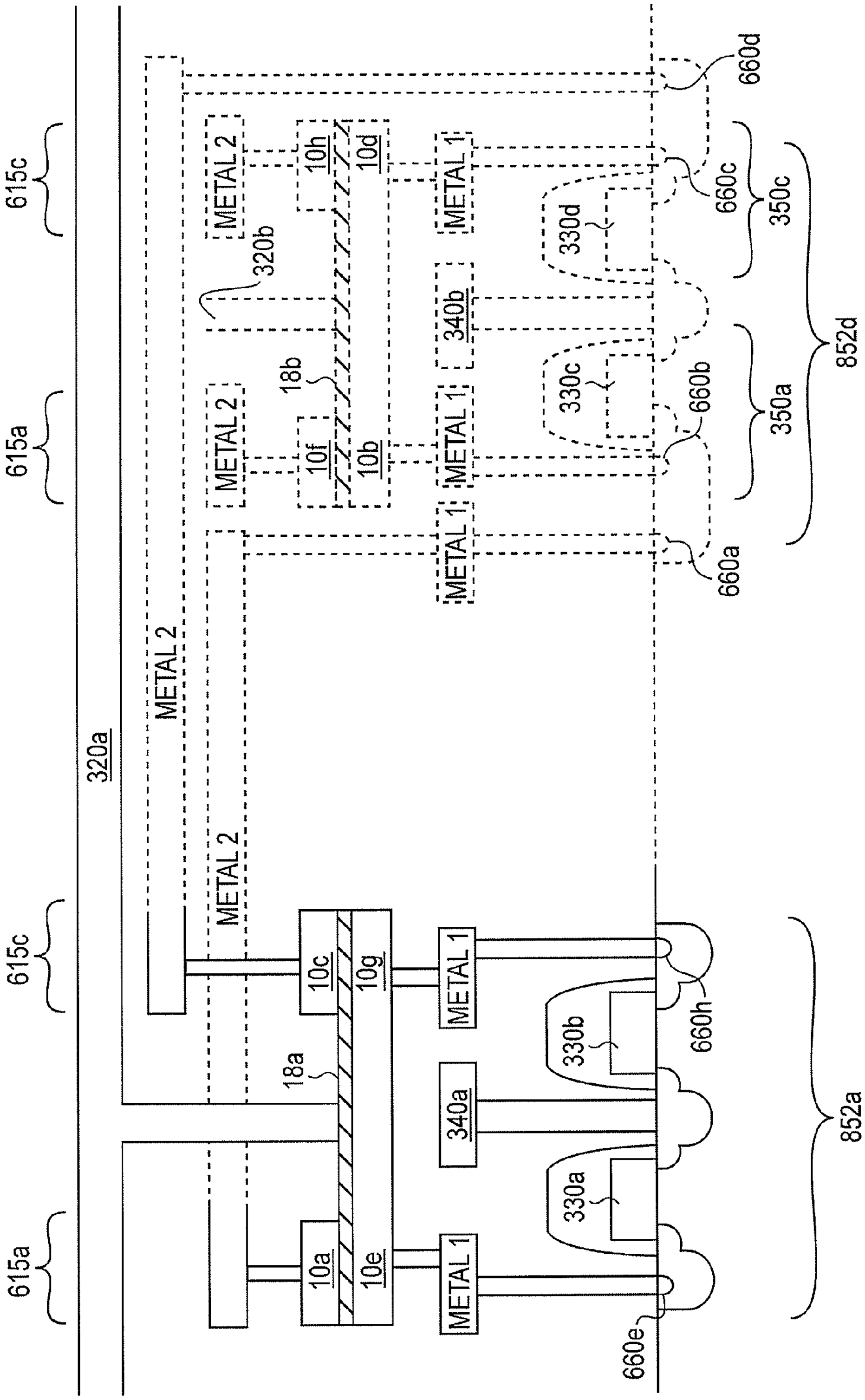

615a
615c
615a
615c
320a
METAL 2
METAL 2
METAL 2
METAL 2
320b
10a
10e
10c
10g
10f
10b
10h
10d
18a
18b
METAL 1
METAL 1
METAL 1
METAL 1
METAL 1
340a
340b
330a
330b
330c
330d
660a
660b
660c
660d
660e
660h
350a
350c
852a
852d

FIG. 7B

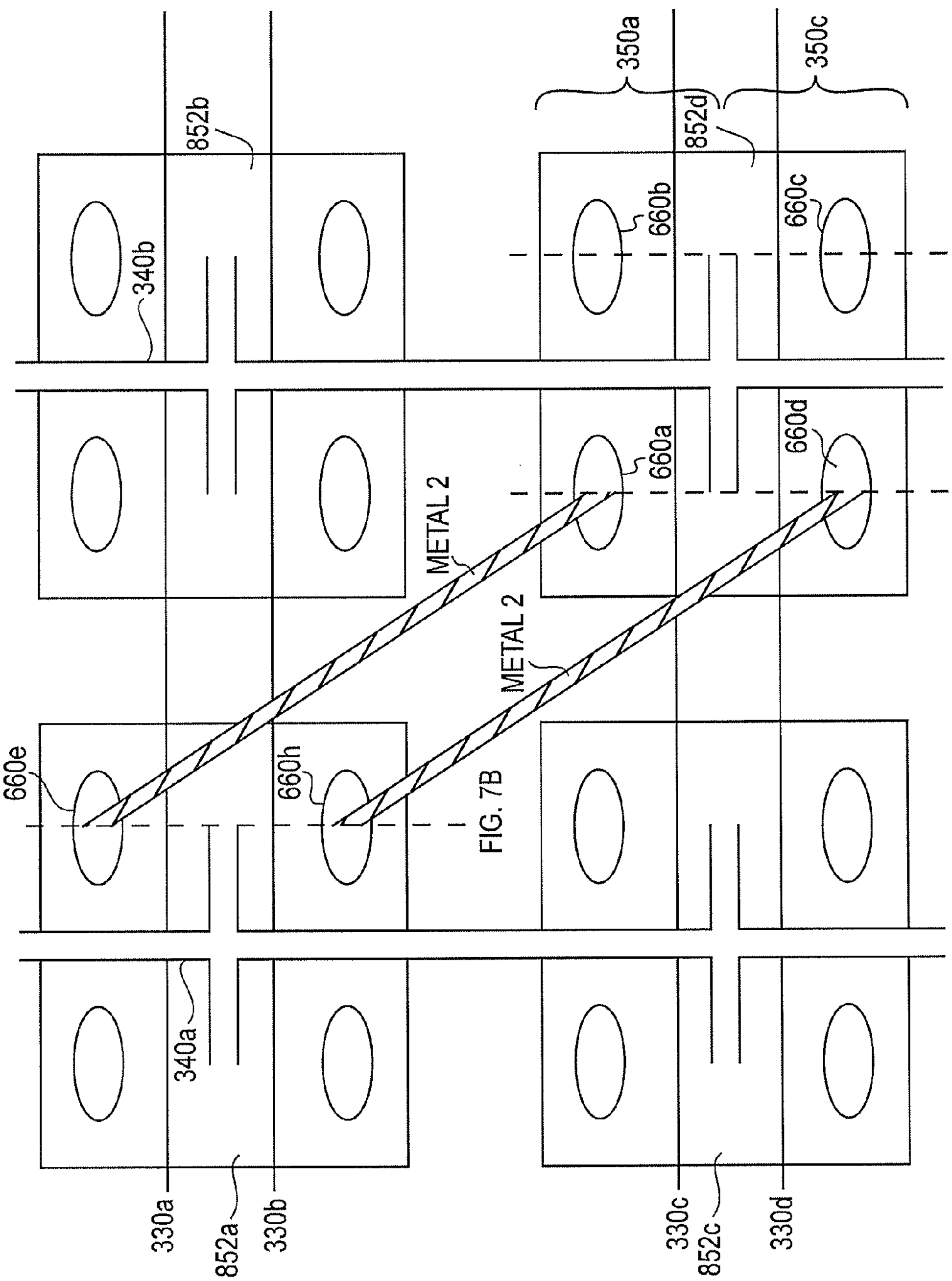

350a
350c
852b
852d
340b
660b
660c
660a
660d
660e
660h
METAL 2
METAL 2
FIG. 7B
FIG. 7B
FIG. 7B
340a
330a
852a
330b
330c
852c
330d

FIG. 7C

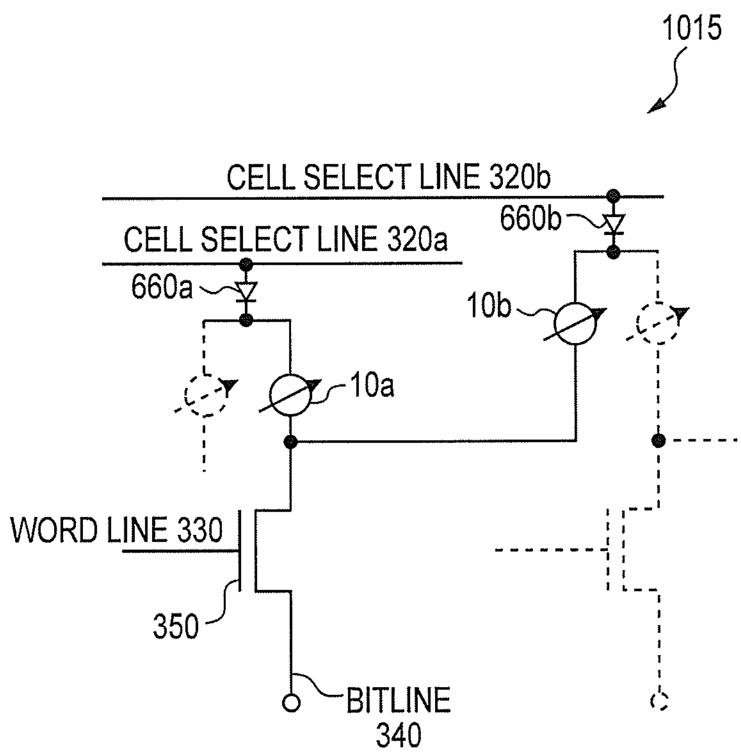

1015
CELL SELECT LINE 320b
660b
CELL SELECT LINE 320a
660a
10b
10a
WORD LINE 330
350
BITLINE
340

FIG. 8A

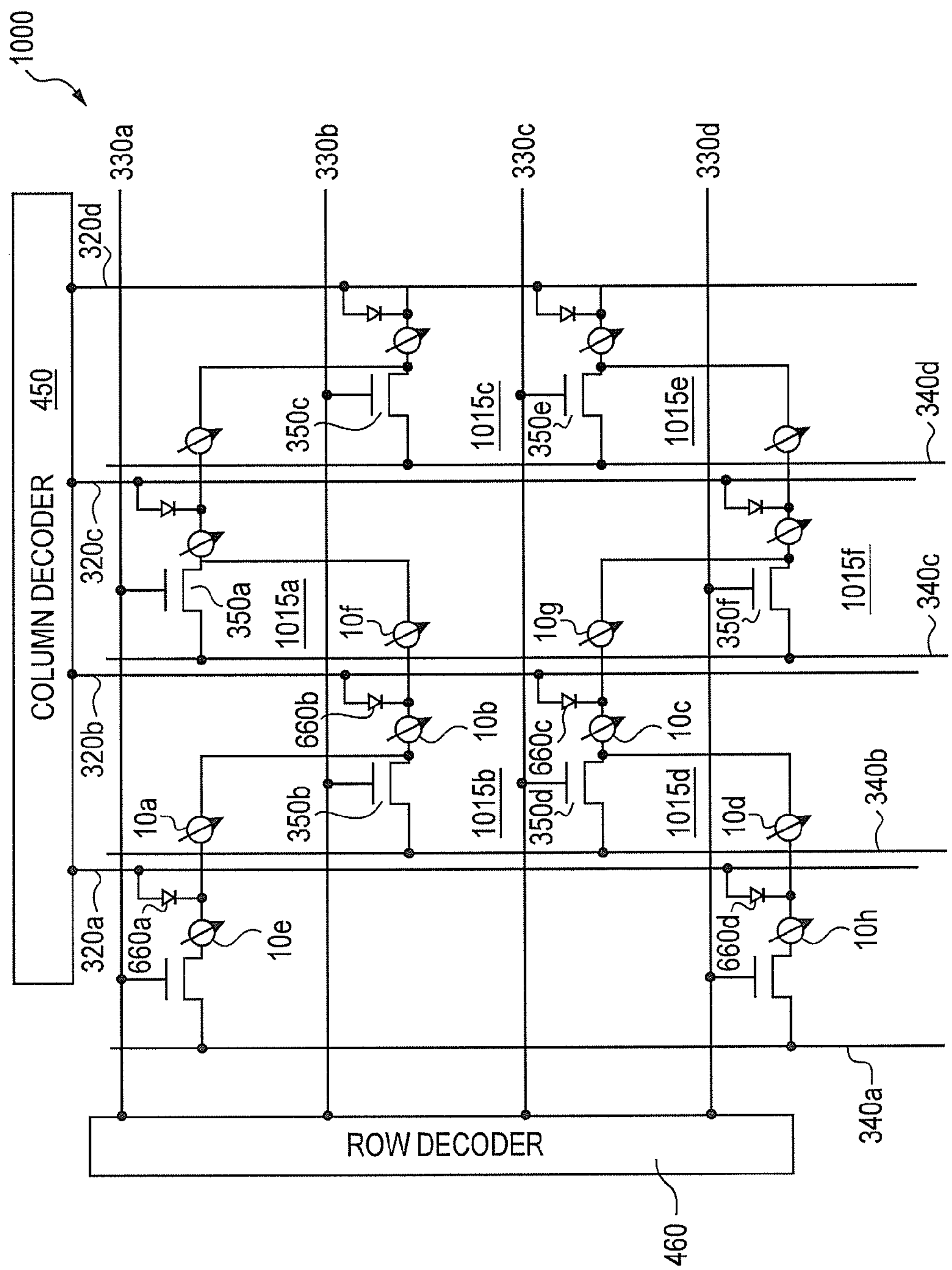
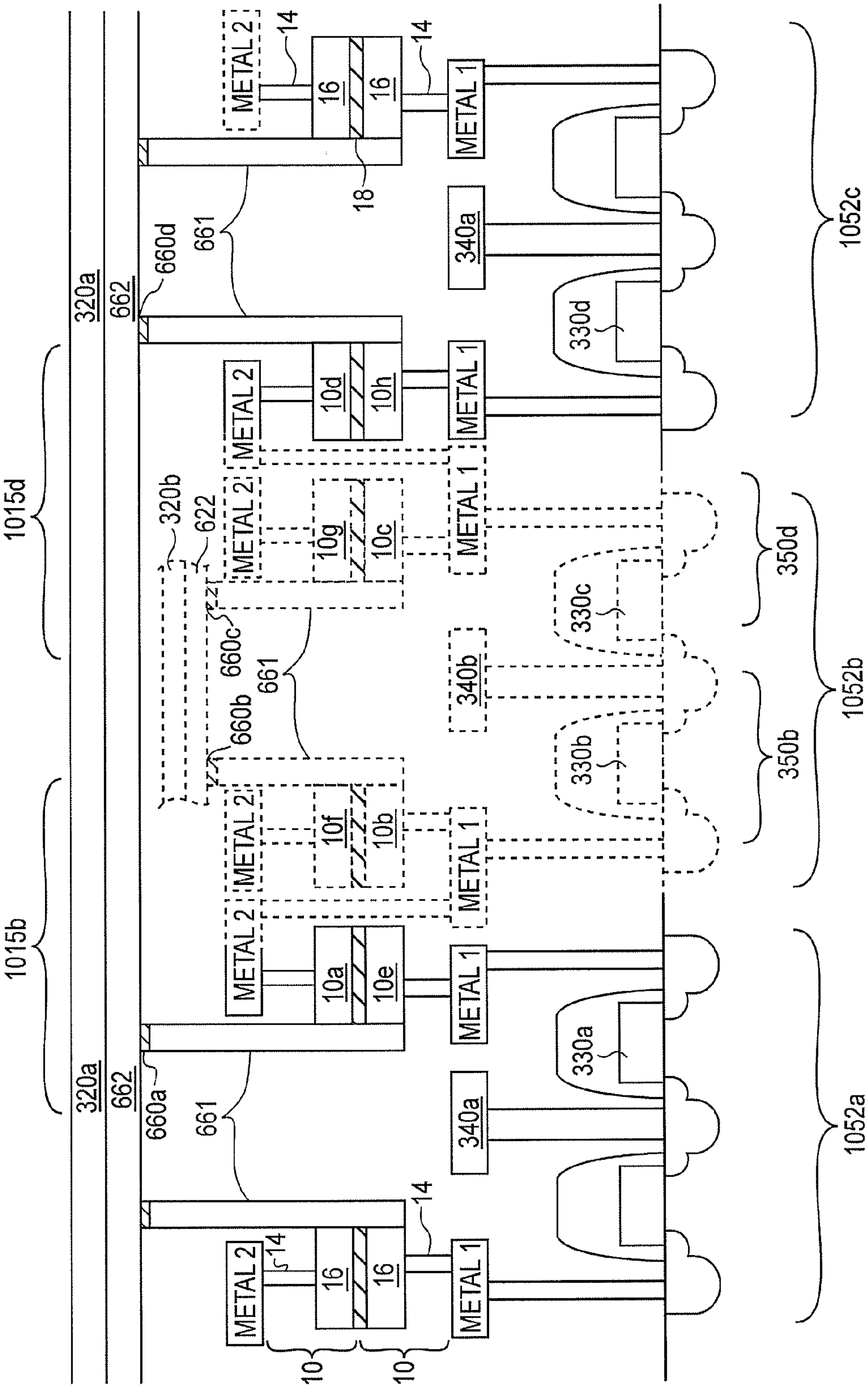

1000
330a
330b
330c
330d
320d
320c
320b
320a
COLUMN DECODER
450
ROW DECODER
460
340a
340b
340c
340d
350a
350b
350c
350d
350e
350f
1015a
1015b
1015c
1015d
1015e
1015f
10a
10b
10c
10d
10e
10f
10g
10h
660a
660b
660c
660d

FIG. 8B



1015d
1015b
320a
662
660d
660a
661
320b
622
660c
660b
METAL 2
METAL 1
14
16
18
10a
10b
10c
10d
10e
10f
10g
10h
340a
340b
330a
330b
330c
330d
350b
350d
1052a
1052b
1052c
10

FIG. 8C

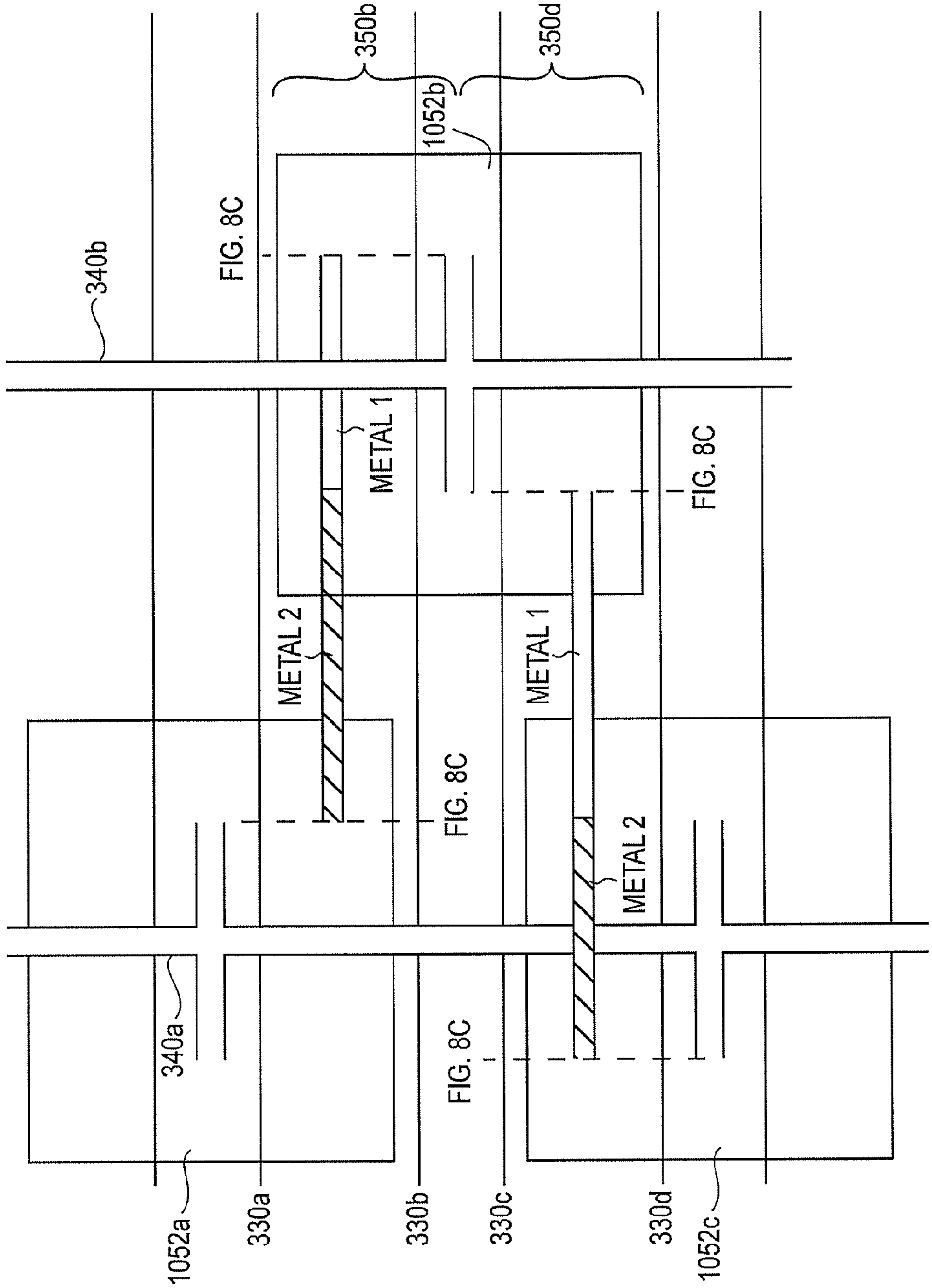

350b
350d
1052b
FIG. 8C
340b
METAL 1
FIG. 8C
METAL 2
METAL 1
FIG. 8C
METAL 2
340a
FIG. 8C
1052a
330a
330b
330c
330d
1052c

FIG. 8D

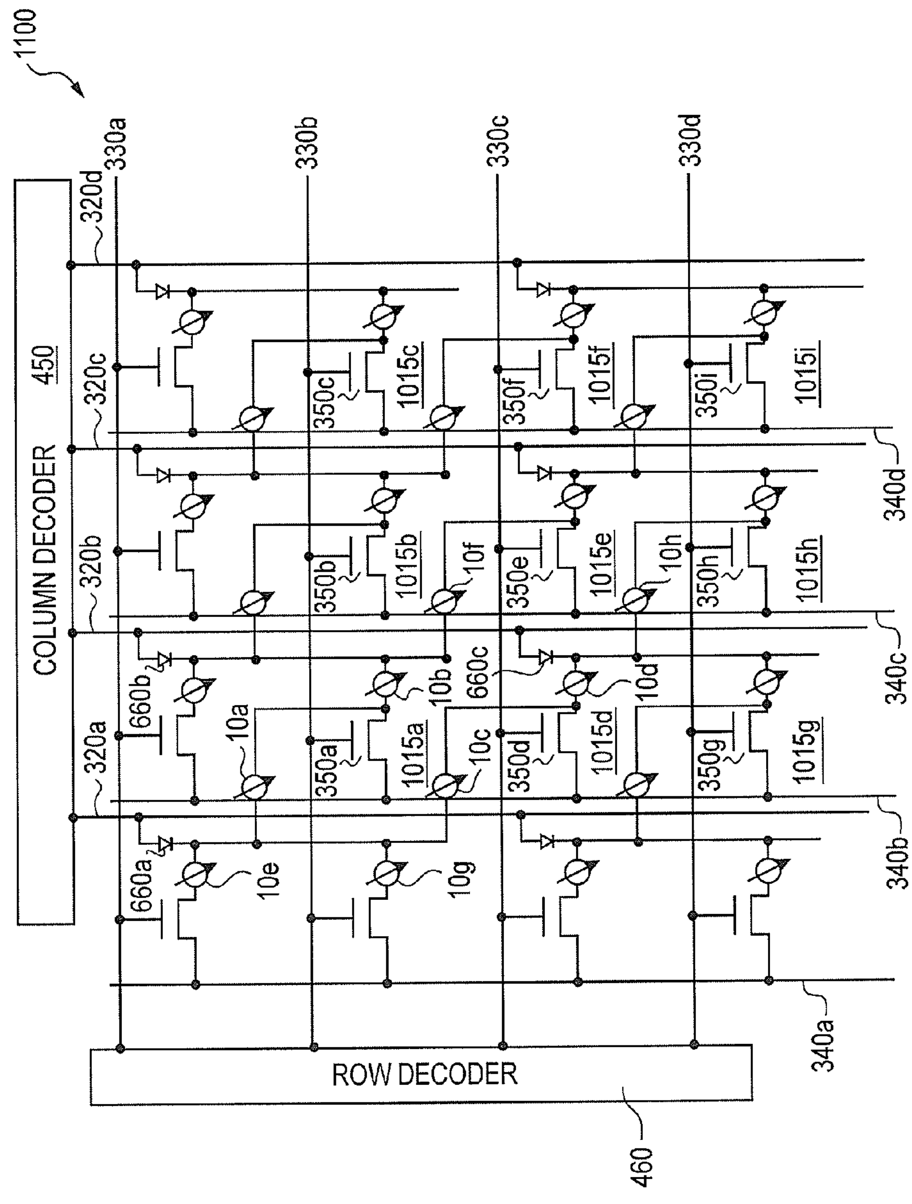

1100
COLUMN DECODER
450
ROW DECODER
460
330a
330b
330c
330d
320a
320b
320c
320d
340a
340b
340c
340d
350a
350b
350c
350d
350e
350f
350g
350h
350i
1015a
1015b
1015c
1015d
1015e
1015f
1015g
1015h
1015i
660a
660b
660c
10a
10b
10c
10d
10e
10f
10g
10h

FIG. 9A

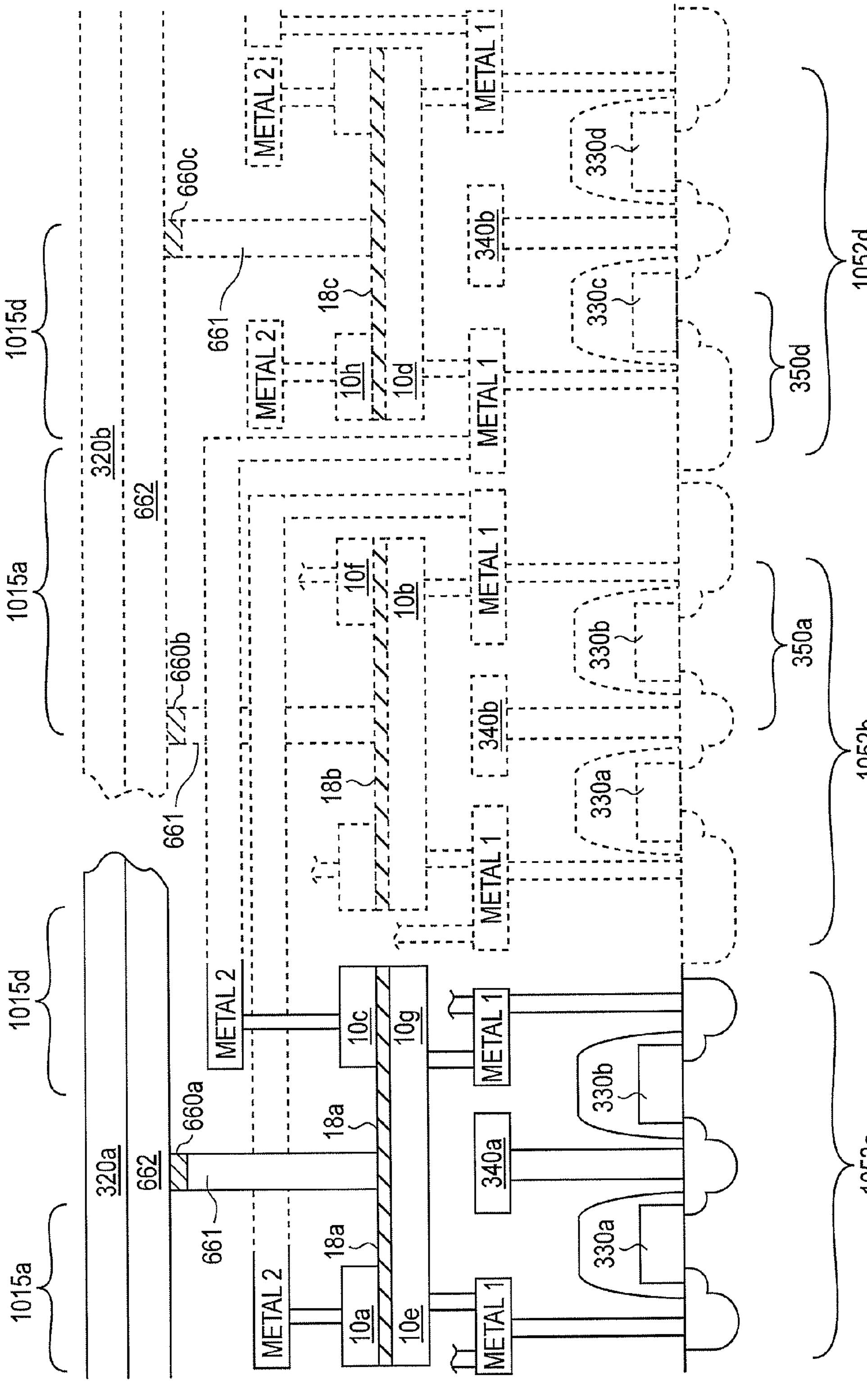

1015a
1015d
1015a
1015d
320a
662
320b
662
660a
661
660b
661
660c
661
METAL 2
METAL 2
METAL 2
METAL 2
10a
10e
18a
18a
10c
10g
10f
10b
18b
10h
10d
18c
METAL 1
METAL 1
METAL 1
METAL 1
METAL 1
METAL 1
340a
340b
340b
330a
330b
330a
330b
330c
330d
350a
350d
1052a
1052b
1052d

FIG. 9B

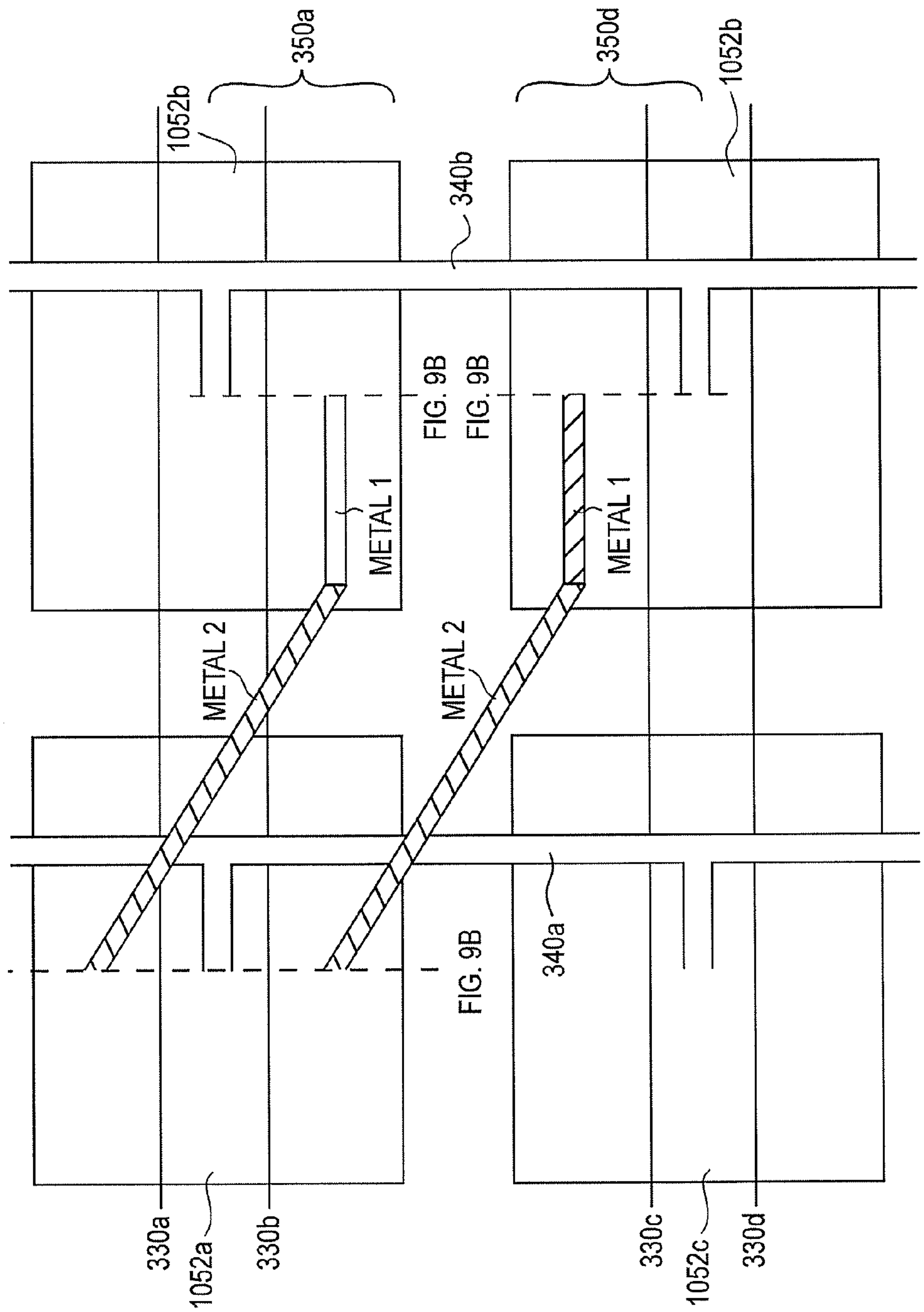

350a
350d
1052b
1052b
340b
FIG. 9B
FIG. 9B
METAL 1
METAL 1
METAL 2
METAL 2
FIG. 9B
340a
330a
1052a
330b
330c
1052c
330d

FIG. 9C

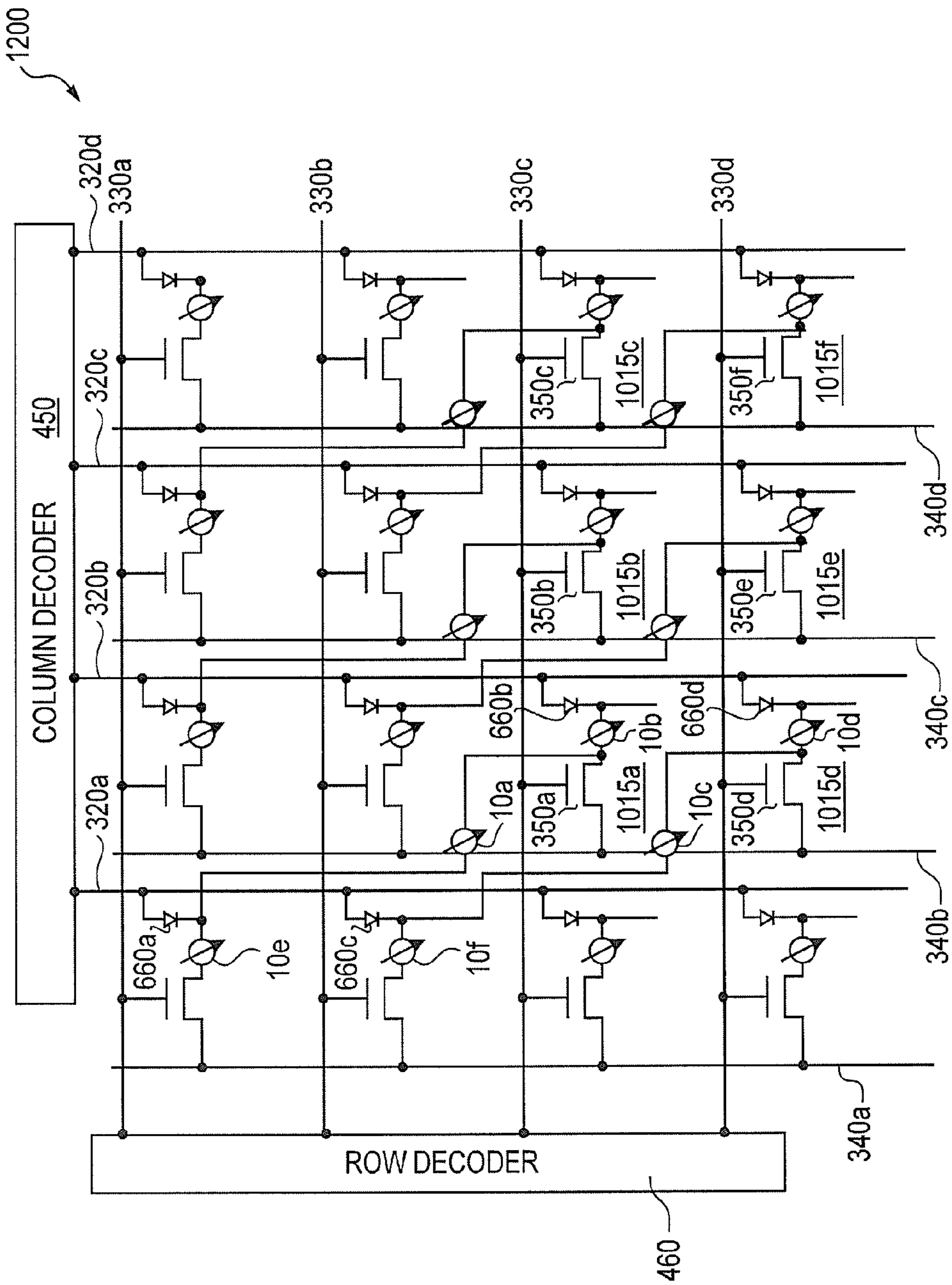

1200
320d
330a
330b
330c
330d
COLUMN DECODER
450
320c
320b
320a
350c
1015c
350f
1015f
350b
1015b
350e
1015e
660b
10b
660d
10d
10a
350a
1015a
10c
350d
1015d
340d
340c
340b
340a
660a
10e
660c
10f
ROW DECODER
460

FIG. 10A

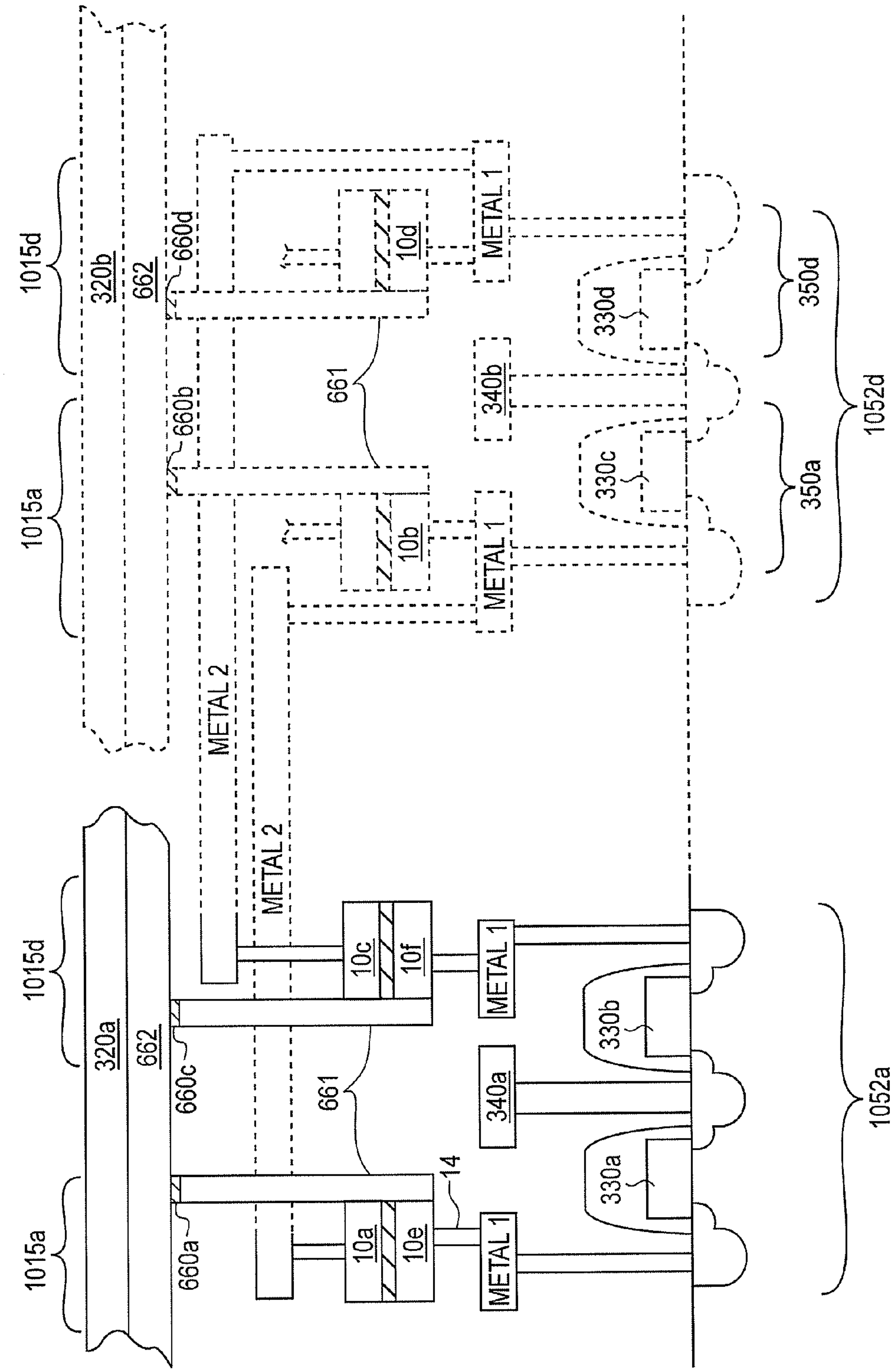

1015a
1015d
320a
662
660a
660c
661
14
10a
10e
10c
10f
METAL 1
METAL 2
340a
330a
330b
1052a
320b
660b
660d
10b
10d
340b
330c
330d
350a
350d
1052d

FIG. 10B

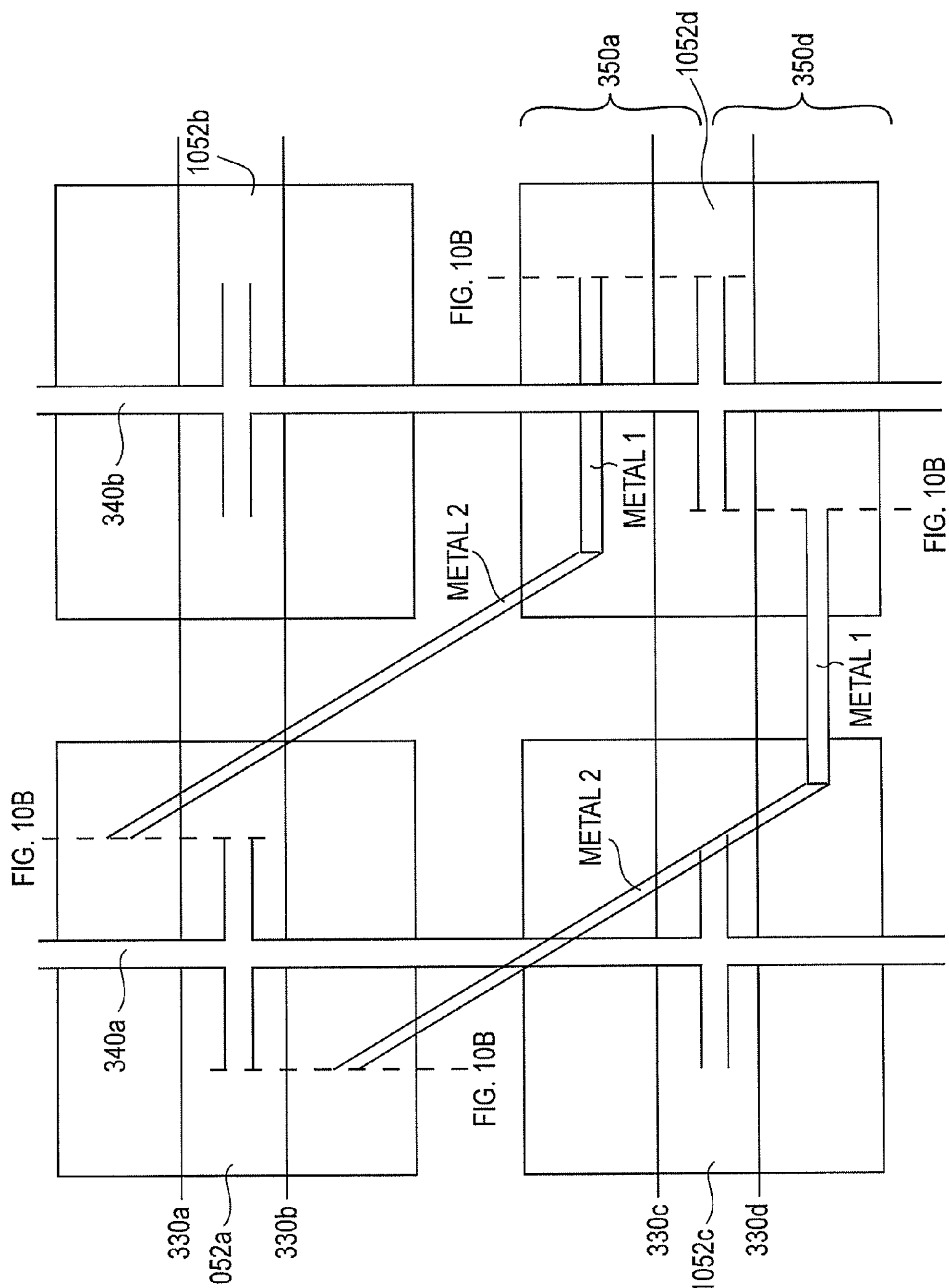

350a
1052d
350d
1052b
FIG. 10B
340b
METAL 1
METAL 2
FIG. 10B
METAL 1
METAL 2
FIG. 10B
340a
FIG. 10B
330a
1052a
330b
330c
1052c
330d

FIG. 10C

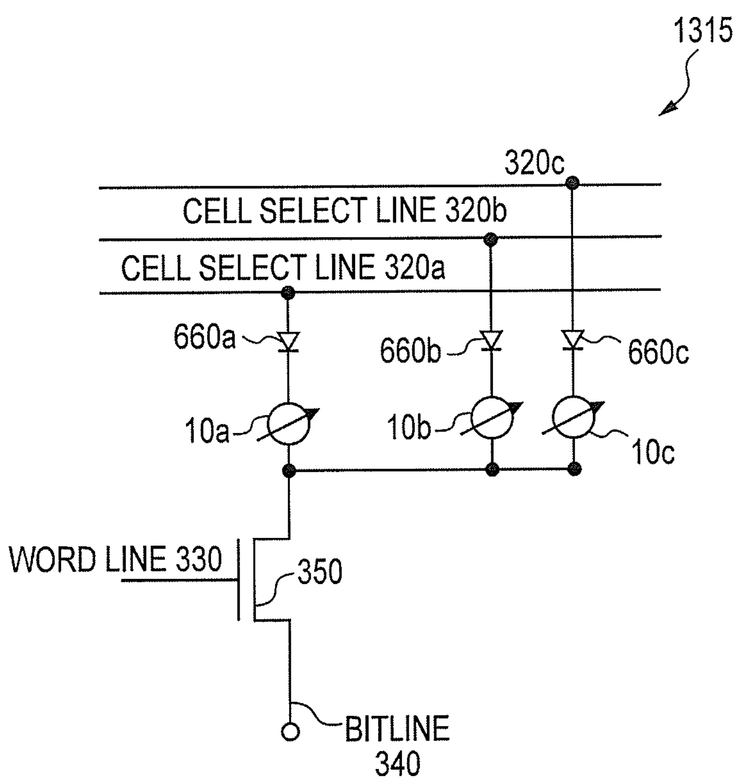

1315
320c
CELL SELECT LINE 320b
CELL SELECT LINE 320a
660a
660b
660c
10a
10b
10c
WORD LINE 330
350
BITLINE
340

FIG. 11A

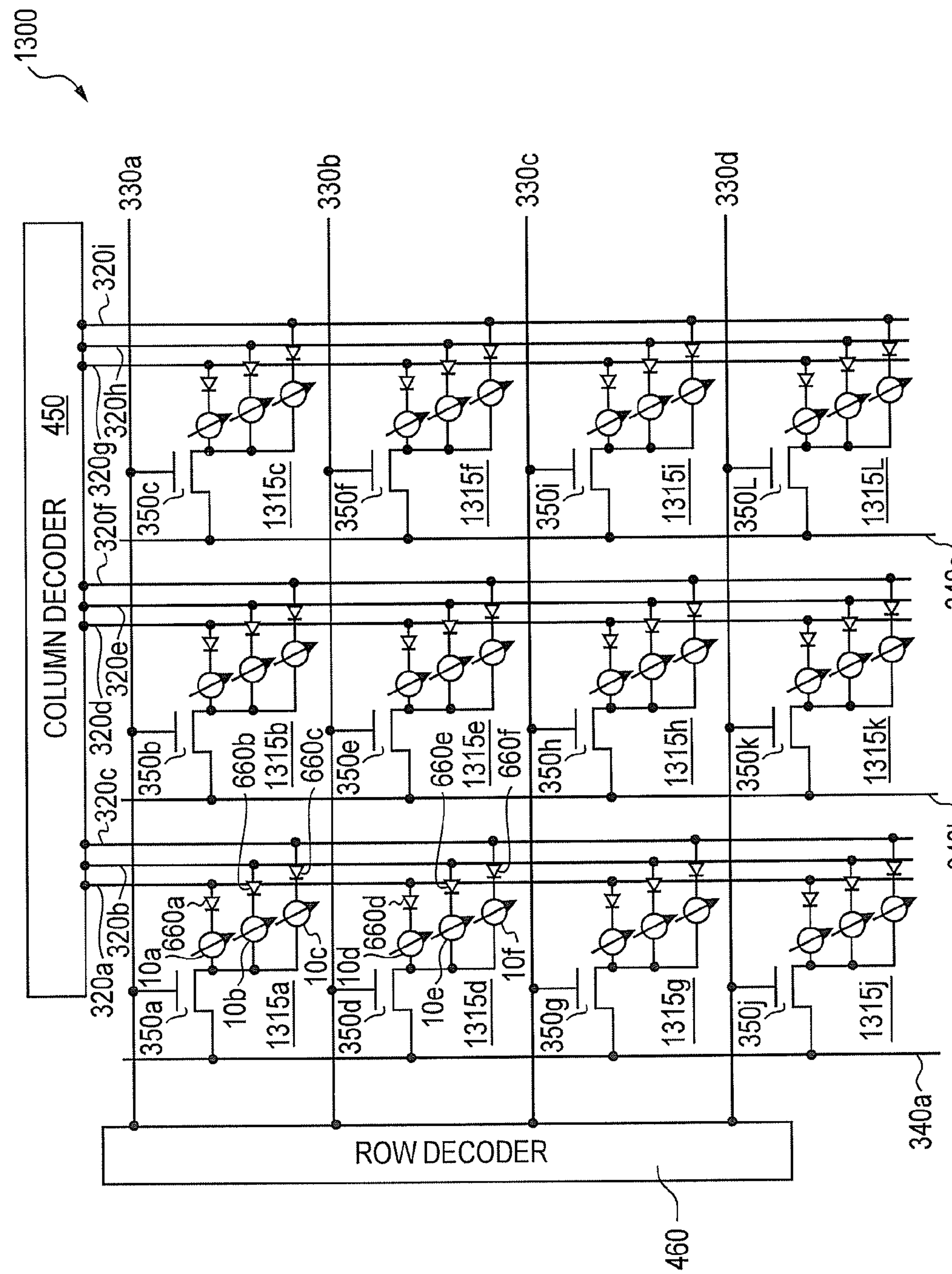

1300
COLUMN DECODER 450
ROW DECODER
460
330a
330b
330c
330d
320a
320b
320c
320d
320e
320f
320g
320h
320i
340a
340b
340c
350a
350b
350c
350d
350e
350f
350g
350h
350i
350j
350k
350L
1315a
1315b
1315c
1315d
1315e
1315f
1315g
1315h
1315i
1315j
1315k
1315L
10a
10b
10c
10d
10e
10f
660a
660b
660c
660d
660e
660f

FIG. 11B

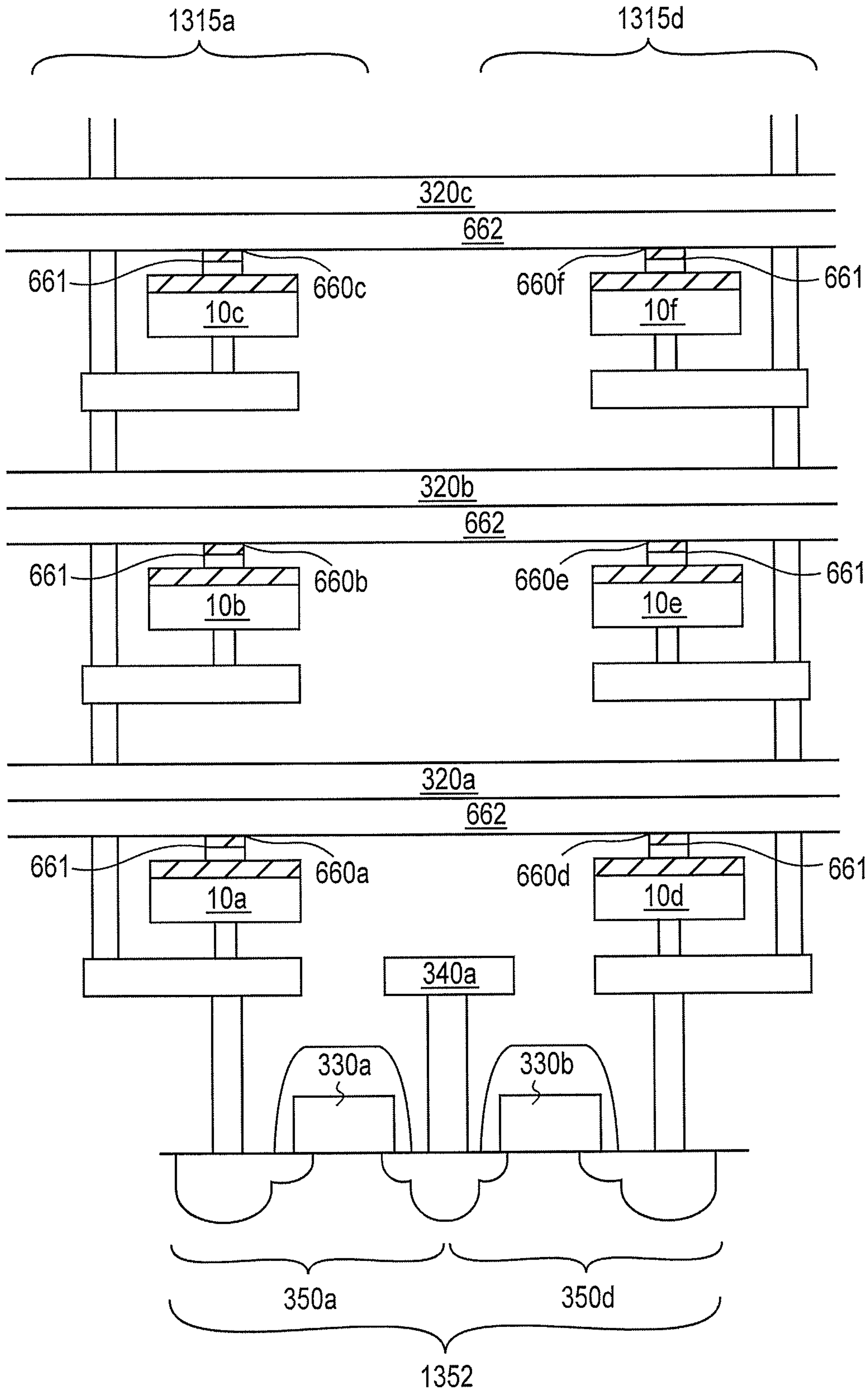

1315a
1315d
320c
662
661
660c
10c
660f
10f
661
320b
662
661
660b
10b
660e
10e
661
320a
662
661
660a
10a
660d
10d
661
340a
330a
330b
350a
350d
1352

FIG. 11C

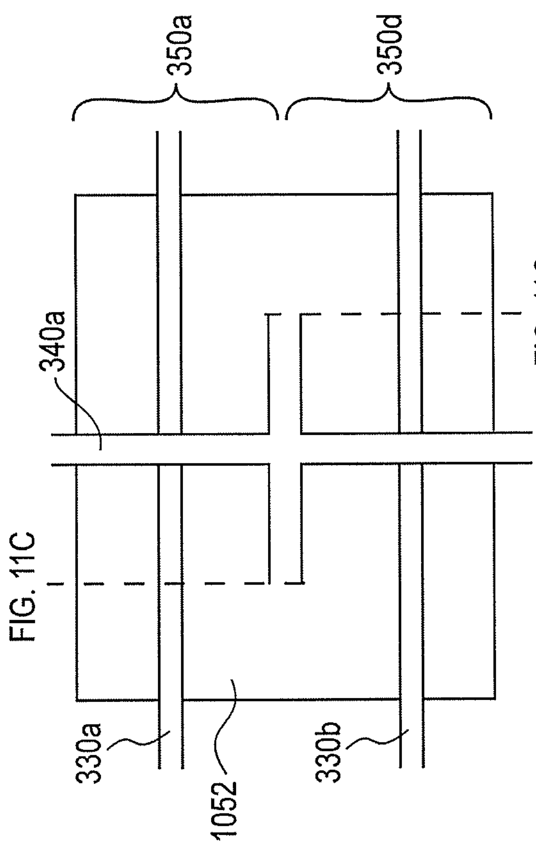


FIG. 11D

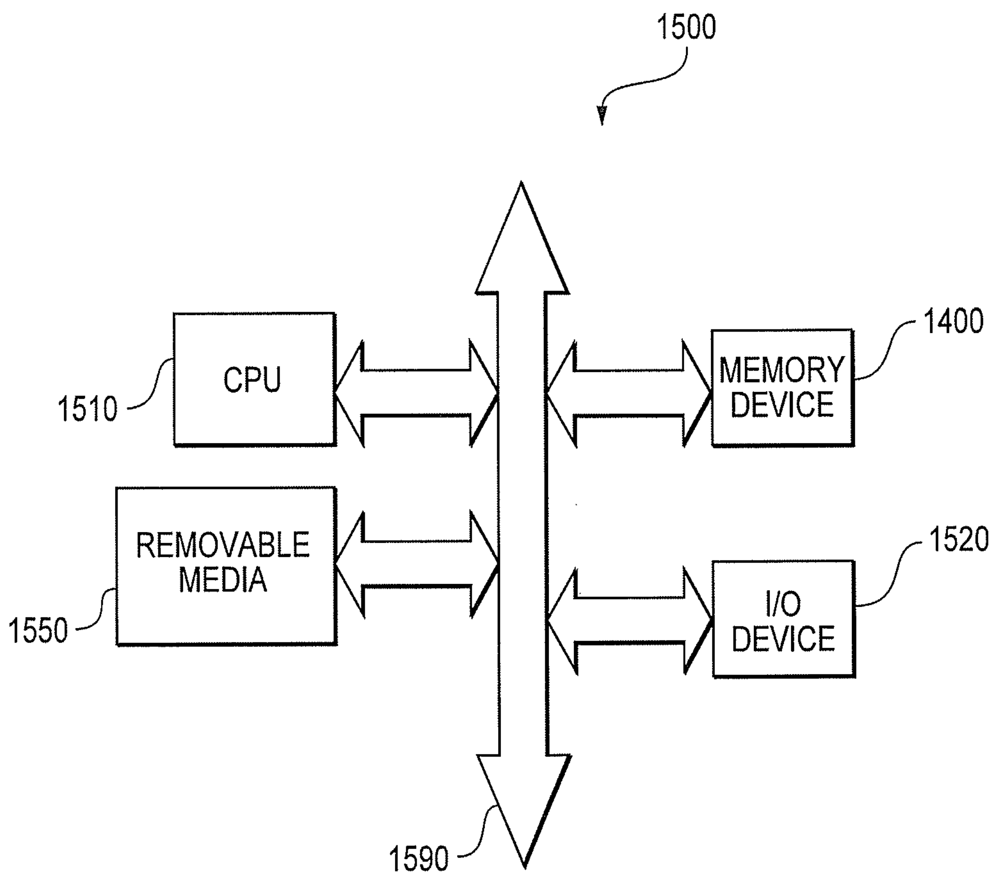

1500
CPU
1510
MEMORY DEVICE
1400
REMOVABLE MEDIA
1550
I/O DEVICE
1520
1590

FIG. 12

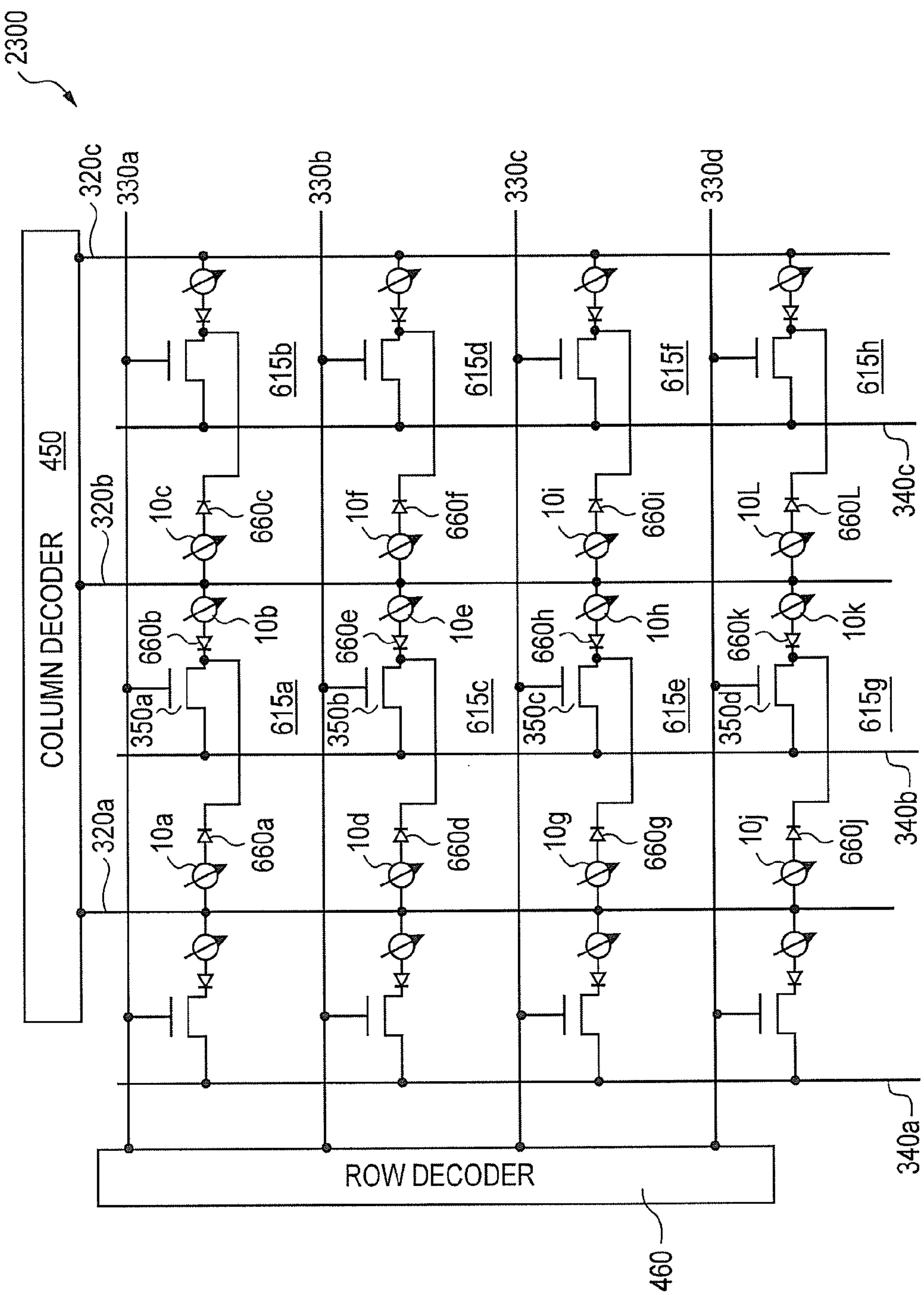

2300
COLUMN DECODER
450
ROW DECODER
460
320a
320b
320c
330a
330b
330c
330d
340a
340b
340c
350a
350b
350c
350d
615a
615b
615c
615d
615e
615f
615g
615h
10a
10b
10c
10d
10e
10f
10g
10h
10i
10j
10k
10L
660a
660b
660c
660d
660e
660f
660g
660h
660i
660j
660k
660L

FIG. 13A

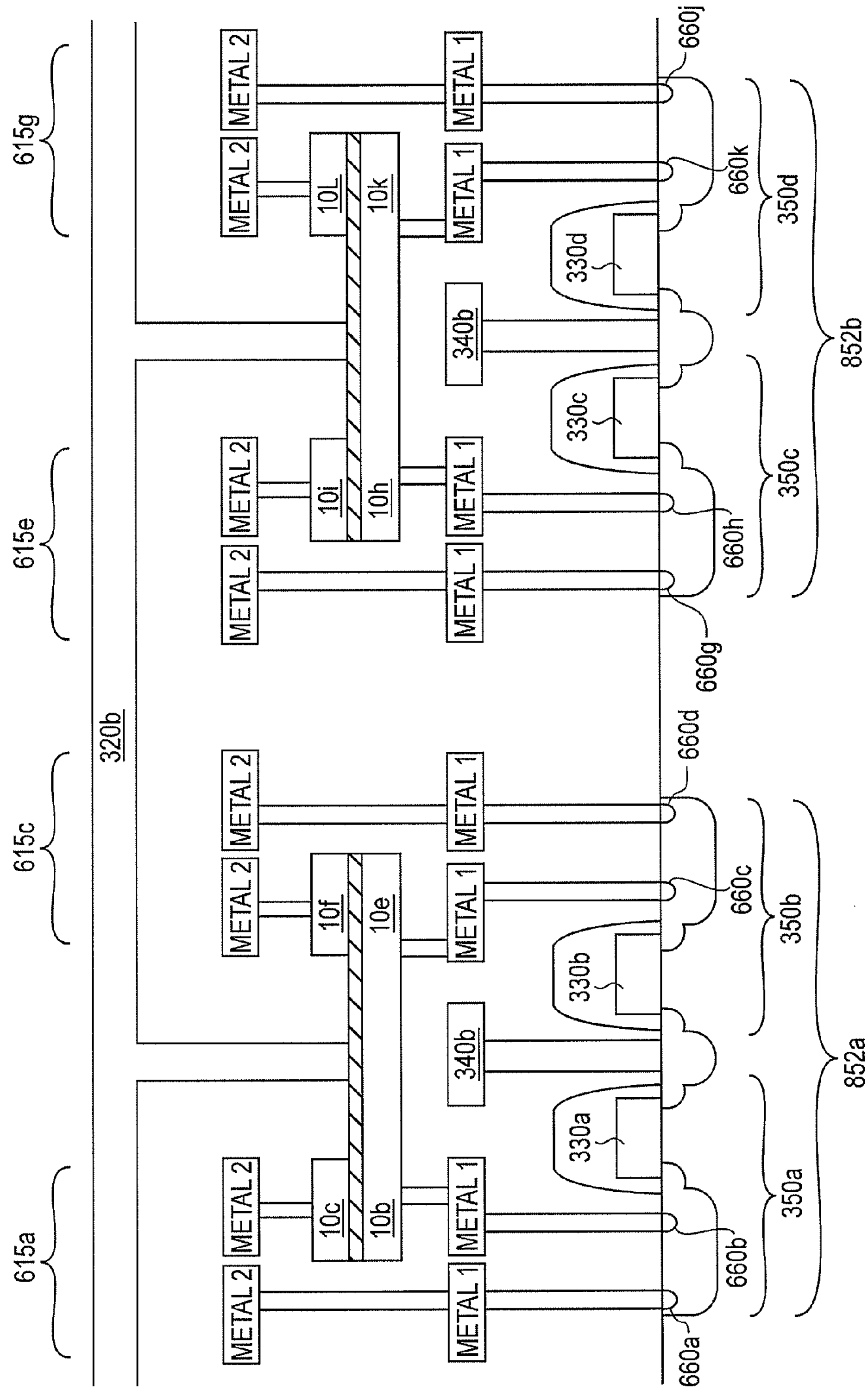

615a
615c
615e
615g
320b
METAL 2
METAL 1
10b
10c
10e
10f
10h
10i
10k
10L
330a
330b
330c
330d
340b
350a
350b
350c
350d
852a
852b
660a
660b
660c
660d
660g
660h
660j
660k

FIG. 13B

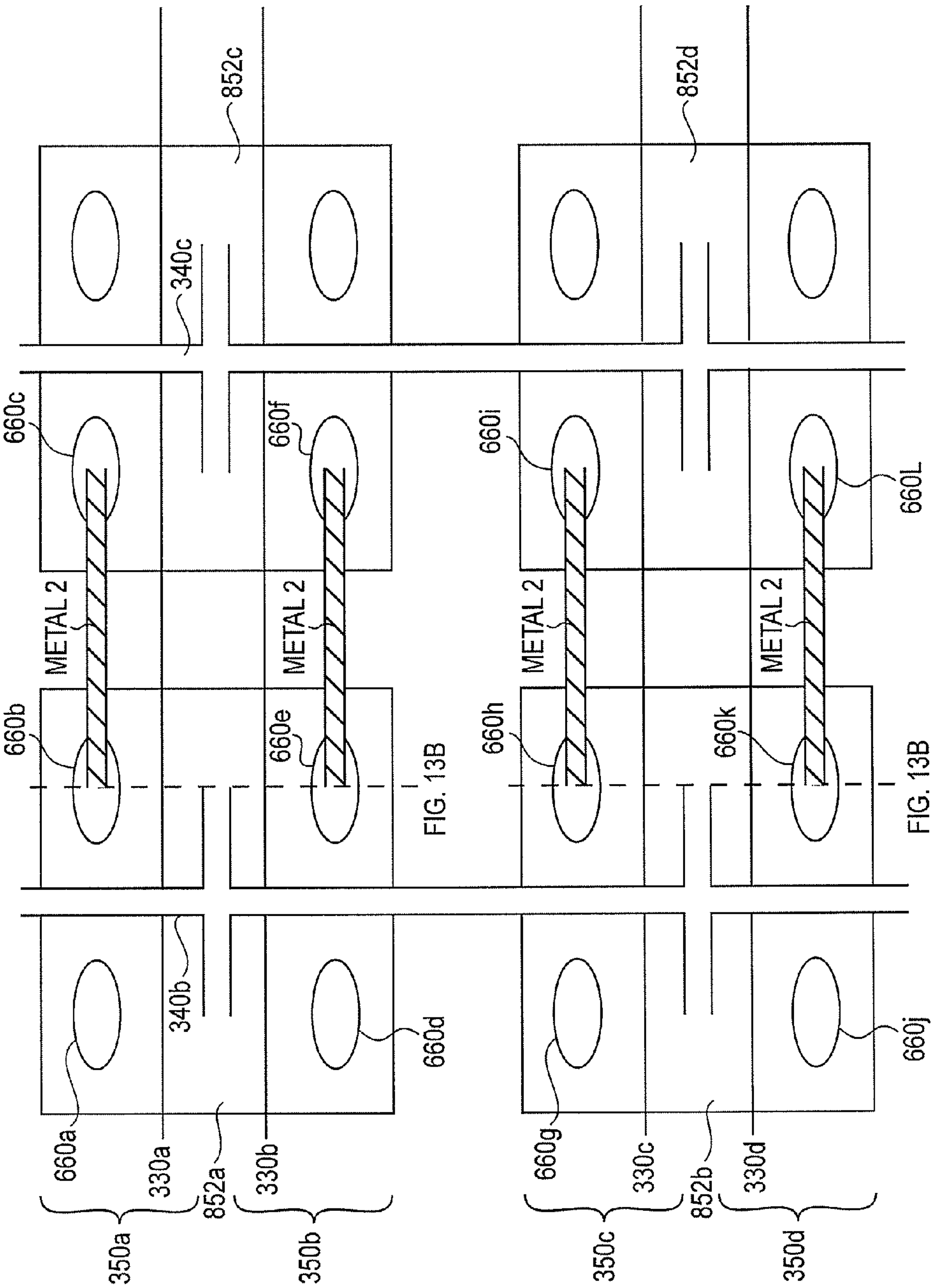

852c
852d
340c
660c
660f
660i
660L
METAL 2
METAL 2
METAL 2
METAL 2
660b
660e
660h
660k
FIG. 13B
FIG. 13B
340b
660d
660j
660a
330a
852a
330b
660g
330c
852b
330d
350a
350b
350c
350d

FIG. 13C

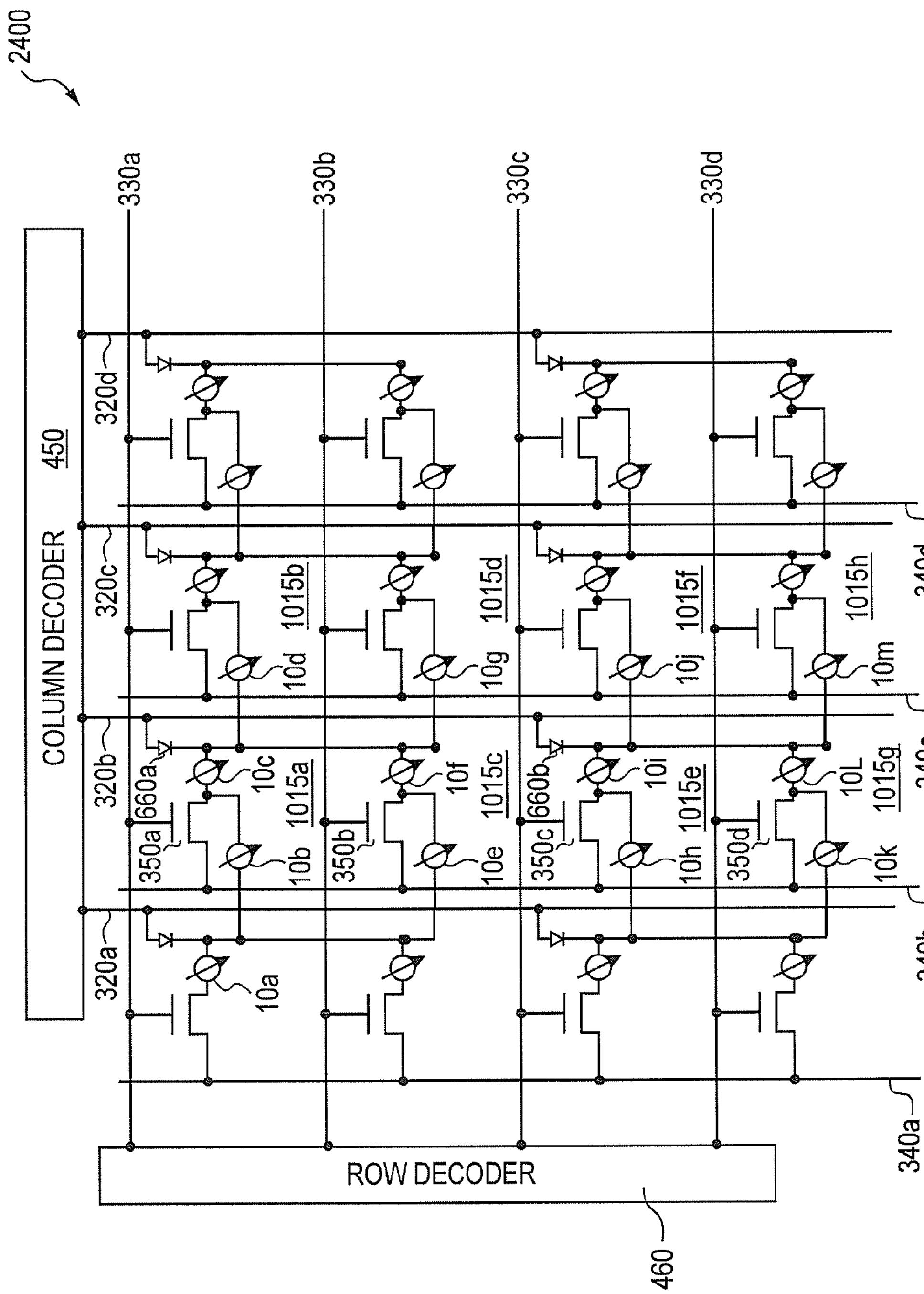

2400
COLUMN DECODER
450
ROW DECODER
460
330a
330b
330c
330d
320a
320b
320c
320d
340a
340b
340c
340d
350a
350b
350c
350d
660a
660b
10a
10b
10c
10d
10e
10f
10g
10h
10i
10j
10k
10L
10m
1015a
1015b
1015c
1015d
1015e
1015f
1015g
1015h

FIG. 14A

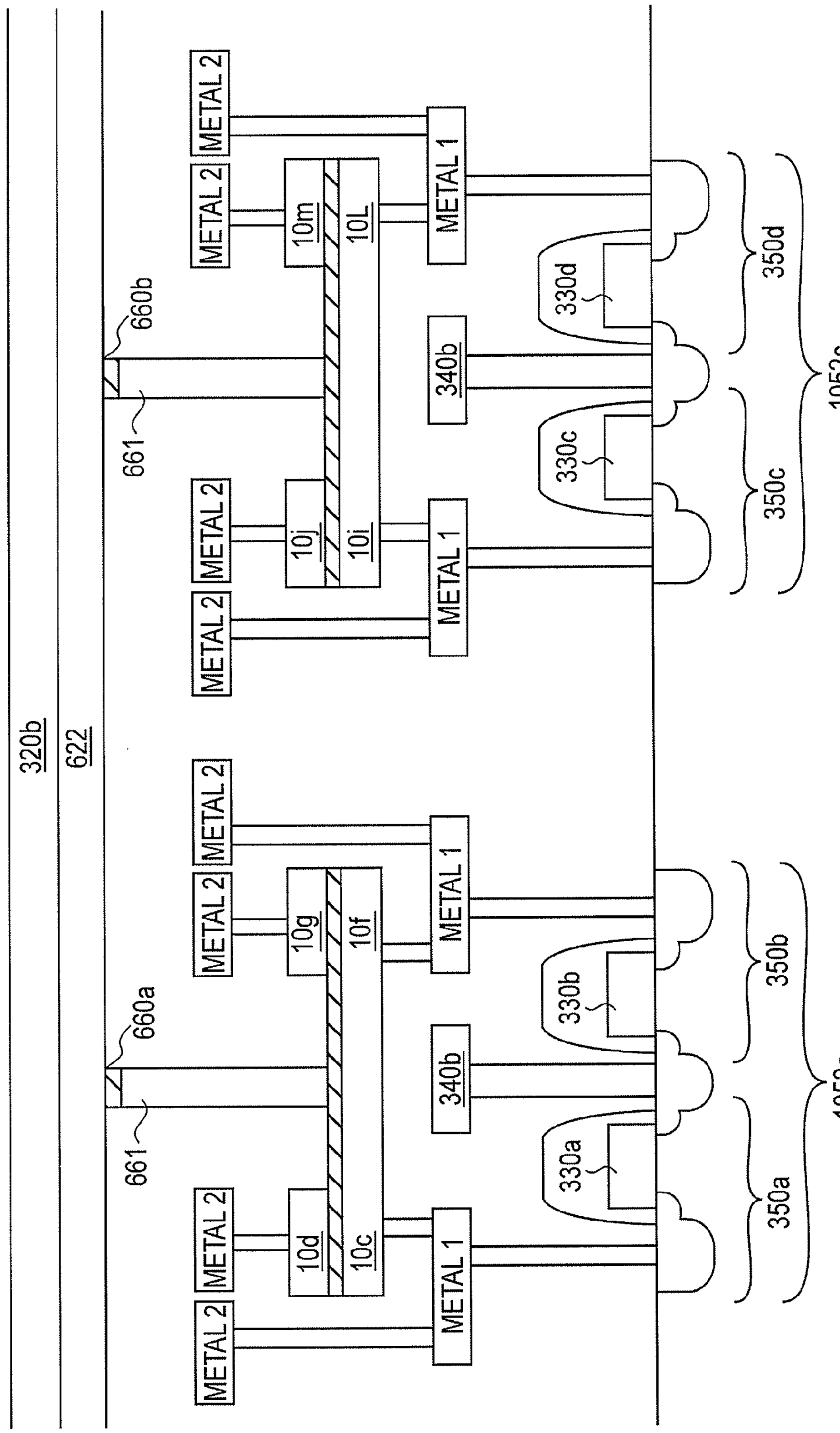

320b
622
660a
660b
661
661
METAL 2
METAL 2
METAL 2
METAL 2
METAL 2
METAL 2
METAL 2
METAL 2
METAL 1
METAL 1
METAL 1
METAL 1
10c
10d
10f
10g
10i
10j
10L
10m
340b
340b
330a
330b
330c
330d
350a
350b
350c
350d
1052a
1052c

FIG. 14B

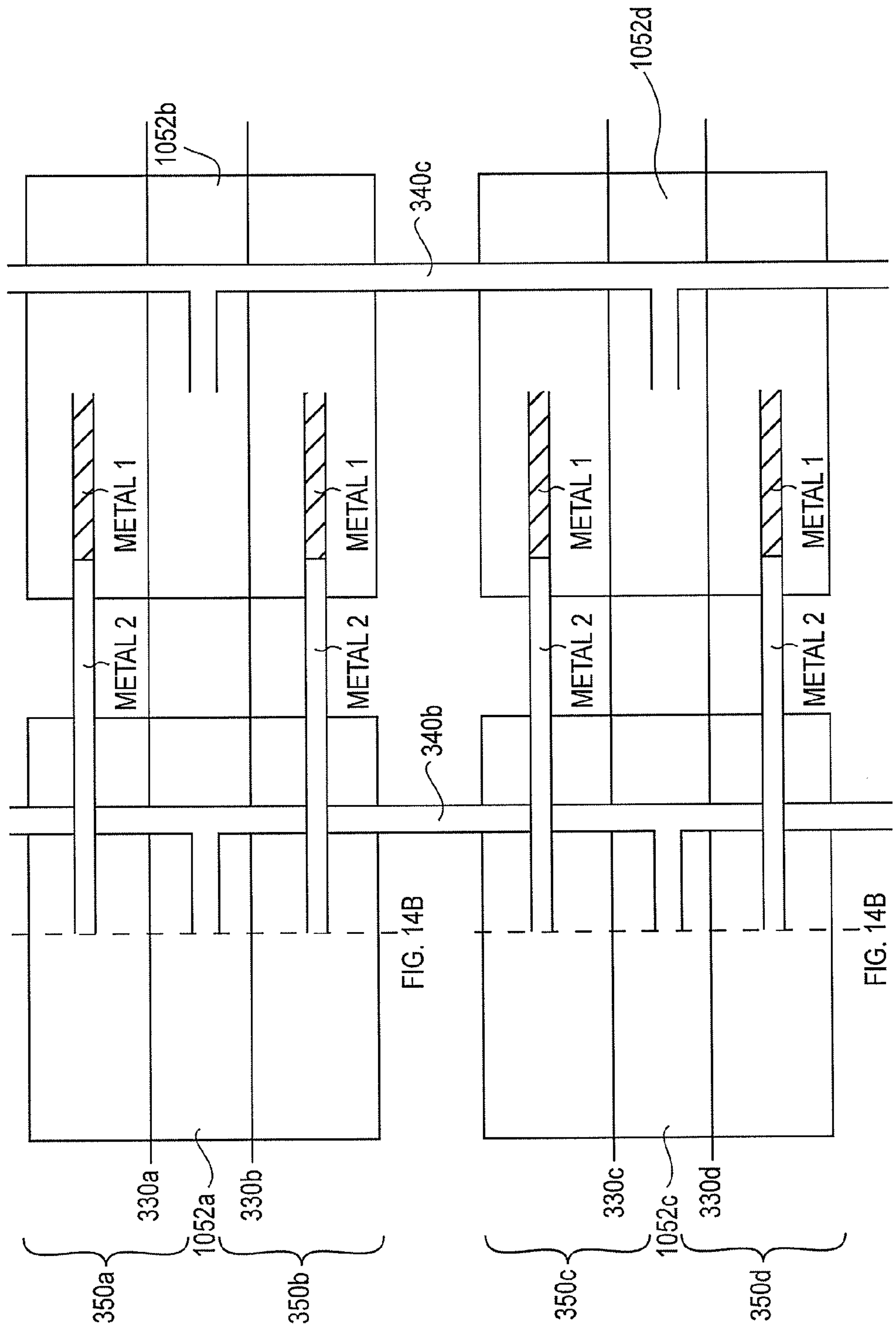

1052b
1052d
340c
METAL 1
METAL 1
METAL 1
METAL 1
METAL 2
METAL 2
METAL 2
METAL 2
340b
FIG. 14B
FIG. 14B
330a
1052a
330b
330c
1052c
330d
350a
350b
350c
350d

FIG. 14C

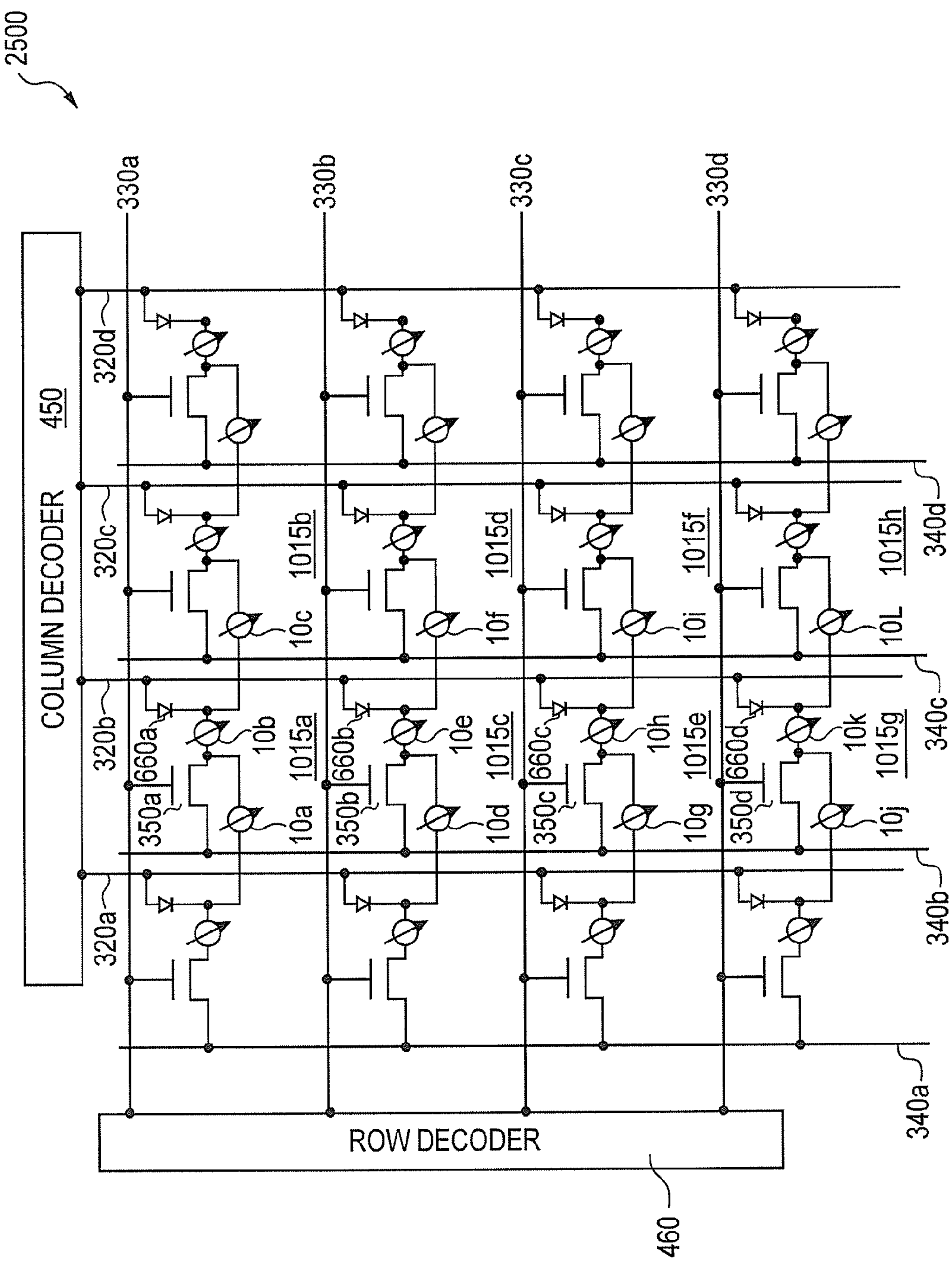

2500
COLUMN DECODER
450
ROW DECODER
460
330a
330b
330c
330d
320a
320b
320c
320d
340a
340b
340c
340d
350a
350b
350c
350d
660a
660b
660c
660d
10a
10b
10c
10d
10e
10f
10g
10h
10i
10j
10k
10L
1015a
1015b
1015c
1015d
1015e
1015f
1015g
1015h

FIG. 15A

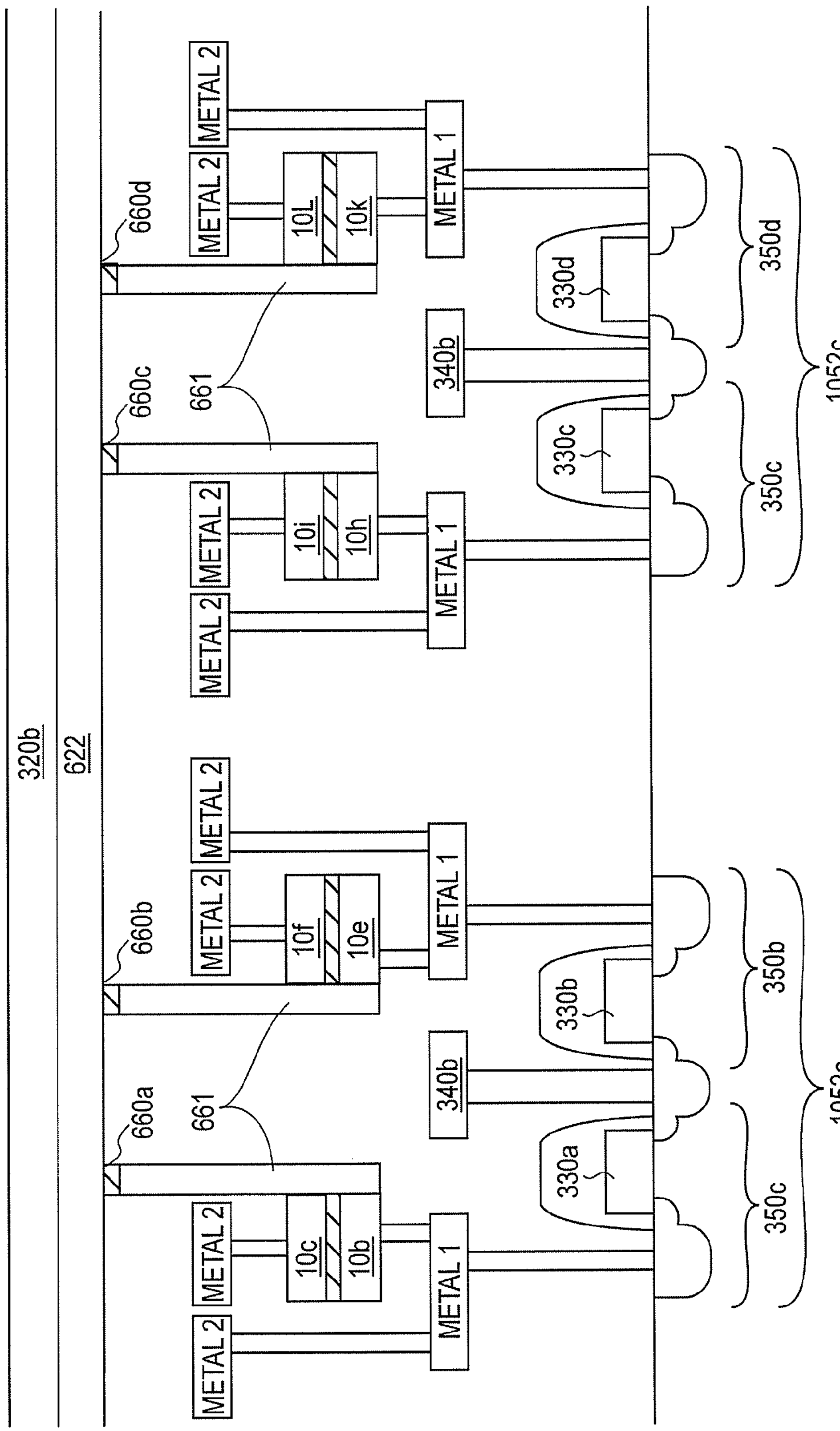
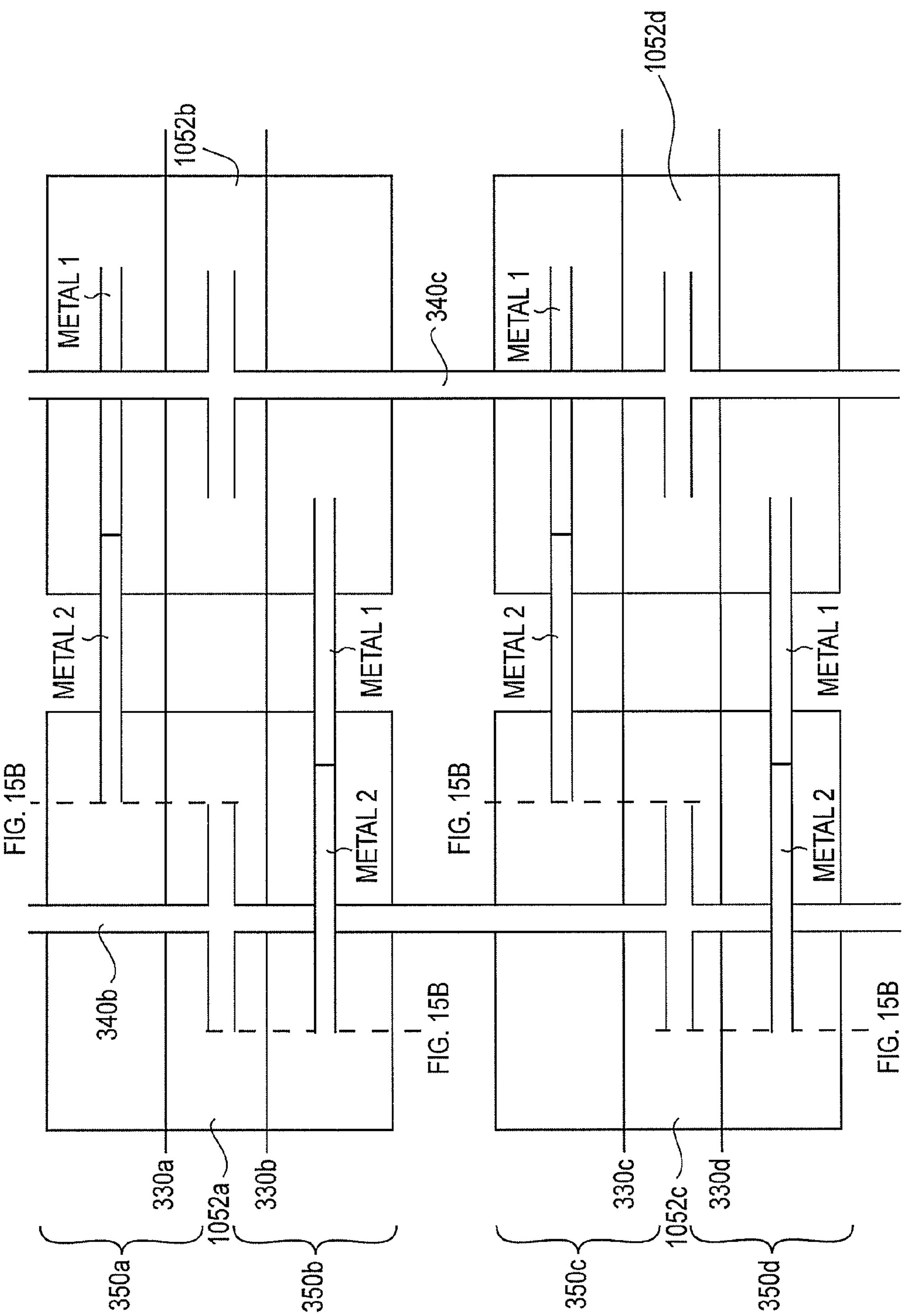

320b
622
660a
660b
660c
660d
661
661
METAL 2
METAL 2
METAL 2
METAL 2
METAL 2
METAL 2
METAL 2
METAL 2
METAL 1
METAL 1
METAL 1
METAL 1
10c
10b
10f
10e
10i
10h
10L
10k
340b
340b
330a
330b
330c
330d
350c
350b
350c
350d
1052a
1052c

FIG. 15B



1052b
1052d
METAL 1
340c
METAL 1
METAL 2
METAL 1
METAL 2
METAL 1
FIG. 15B
FIG. 15B
METAL 2
METAL 2
340b
FIG. 15B
FIG. 15B
330a
1052a
330b
330c
1052c
330d
350a
350b
350c
350d

FIG. 15C

RESISTIVE MEMORY ARCHITECTURES WITH MULTIPLE MEMORY CELLS PER ACCESS DEVICE

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a divisional application of U.S. patent application Ser. No. 13/292,884, filed Nov. 9, 2011, which is continuation of U.S. patent application Ser. No. 12/656,720, filed Feb. 16, 2010, now U.S. Pat. No. 8,076,195, issued Dec. 13, 2011, which is a divisional of U.S. patent application Ser. No. 11/806,495, filed May 31, 2007, now U.S. Pat. No. 7,684,227, issued Mar. 23, 2010, the specifications of each of which are herein incorporated by reference in their entirety.

FIELD OF THE INVENTION

The embodiments of the invention relate generally to the field of semiconductor devices and, more particularly, to resistive memory devices, e.g., phase change memory devices.

BACKGROUND OF THE INVENTION

Microprocessor-accessible memory devices have traditionally been classified as either non-volatile or volatile memory devices. Non-volatile memory devices are capable of retaining stored information even when power to the memory device is turned off. Traditionally, however, non-volatile memory devices occupy a large amount of space and consume large quantities of power, making these devices unsuitable for use in portable devices or as substitutes for frequently-accessed volatile memory devices. On the other hand, volatile memory devices tend to provide greater storage capability and programming options than non-volatile memory devices. Volatile memory devices also generally consume less power than non-volatile devices. However, volatile memory devices require a continuous power supply in order to retain stored memory content.

Research and development of commercially viable memory devices that are randomly accessed, have relatively low power consumption, and are non-volatile is ongoing. One ongoing area of research is in resistive memory cells where resistance states can be programmably changed. One avenue of research relates to devices that store data in memory cells by structurally or chemically changing a physical property of the memory cells in response to applied programming voltages, which in turn change cell resistance. Examples of variable resistance memory devices being investigated include memories using variable resistance polymers, perovskite, doped amorphous silicon, phase-changing glasses, and doped chalcogenide glass, among others.

FIG. **1** shows a basic composition of a typical variable resistance memory cell such as a phase change memory cell **10** constructed over a substrate **12**, having a variable resistance material, e.g., a phase change material **16** formed between a bottom electrode **14** and a top electrode **18**. One type of variable resistance material may be amorphous silicon doped with V, Co, Ni, Pd, Fe and Mn as disclosed in U.S. Pat. No. 5,541,869 to Rose et al. Another type of variable resistance material may include perovskite materials such as $Pr_{(1-x)}Ca_xMnO_3$ (PCMO), $La_{(1-x)}Ca_xMnO_3$ (LCMO), $LaSrMnO_3$ (LSMO), $GdBaCo_xO_y$ (GBCO) as disclosed in U.S. Pat. No. 6,473,332 to Ignatiev et al. Still another type of variable resistance material may be a doped chalcogenide glass of the formula A_xB_y, where "B" is selected from among S, Se and Te and mixtures thereof, and where "A" includes at least one element from Group III-A (B, Al, Ga, In, Tl), Group IV-A (C, Si, Ge, Sn, Pb), Group V-A (N, P, As, Sb, Bi), or Group VII-A (F, Cl, Br, I, At) of the periodic table, and with the dopant being selected from among the noble metals and transition metals, including Ag, Au, Pt, Cu, Cd, Ir, Ru, Co, Cr, Mn or Ni, as disclosed in U.S. Pat. Nos. 6,881,623 and 6,888,155 to Campbell et al. and Campbell, respectively. Yet another type of variable resistance material includes a carbon-polymer film comprising carbon black particulates or graphite, for example, mixed into a plastic polymer, such as that disclosed in U.S. Pat. No. 6,072,716 to Jacobson et al. The material used to form the electrodes **14**, **18** can be selected from a variety of conductive materials, such as tungsten, nickel, tantalum, titanium, titanium nitride, aluminum, platinum, or silver, among others.

Much research has focused on memory devices using memory elements composed of chalcogenides. Chalcogenides are alloys of Group VI elements of the periodic table, such as Te or Se. A specific chalcogenide currently used in rewriteable compact discs ("CD-RWs") is $Ge_2Sb_2Te_5$. In addition to having valuable optical properties that are utilized in CD-RW discs, $Ge_2Sb_2Te_5$ also has desirable physical properties as a variable resistance material. Various combinations of Ge, Sb and Te may be used as variable resistance materials and which are herein collectively referred to as GST materials. Specifically, GSTs can change structural phases between an amorphous phase and two crystalline phases. The resistance of the amorphous phase ("a-GST") and the resistances of the cubic and hexagonal crystalline phases ("c-GST" and "h-GST," respectively) can differ significantly. The resistance of amorphous GST is greater than the resistances of either cubic GST or hexagonal GST, whose resistances are similar to each other. Thus, in comparing the resistances of the various phases of GST, GST may be considered a two-state material (amorphous GST and crystalline GST), with each state having a different resistance that can be equated with a corresponding binary state. A variable resistance material such as GST whose resistance changes according to its material phase is referred to as a phase change material.

The transition from one GST phase to another occurs in response to temperature changes of the GST material. The temperature changes, i.e., the heating and cooling, can be caused by passing differing amounts of current through the GST material. The GST material is placed in a crystalline state by passing a crystallizing current through the GST material, thus warming the GST material to a temperature wherein a crystalline structure may grow. A stronger melting current is used to melt the GST material for subsequent cooling to an amorphous state. As the typical phase change memory cell uses the crystalline state to represent one logical state binary, e.g., "1," and the amorphous state to represent another logical state binary, e.g., "0," the crystallizing current is referred to as a set current I_{SET} and the melting current is referred to as an erase or reset current I_{RST}. One skilled in the art will understand, however, that the assignment of GST states to binary values may be switched if desired. The set currents I_{SET} and the erase or reset currents I_{RST} are typically large, often in the order of a few hundred microamps.

A typical resistive memory bit structure such as a phase change memory bit structure **315** that incorporates a phase change memory cell **10**, for example, is represented schematically in FIG. **2**A. In FIG. **2**A, the memory cell **10** is connected to a cell select line **320** via either the cell's top or bottom electrode. The opposing electrode is connected to an access device **350** such as an access transistor. The access device **350** is gated by a word line **330**. A bit line **340** provides a source to the access device **350** and is connected to the memory cell **10** when the access device **350** is activated by the word line **330**. The access device **350** must be sufficiently large in order to pass the large phase changing currents I_{SET} and I_{RST} to the memory cell **10**.

The memory bit structure **315** of FIG. **2**A may be arranged into an array of memory bit structures, as illustrated in FIG. **2**B. In FIG. **2**B, a conventional resistive memory device **400** includes an array of memory bit structures **315***a*-**315***h*. The memory bit structures **315***a*-**315***h* are arranged in rows and columns. The rows and columns may be partially staggered, as in FIG. **2**B, or may be aligned in parallel. The memory bit structures **315***a*-**315***h* along any given cell select line **320***a*-**320***d* do not share a common word line **330***a*-**330***d*. Additionally, the memory bit structures **315***a*-**315***h* along any given word line **330***a*-**330***d* do not share a common bit line **340***a*-**340***d*. In this manner, each memory bit structure is uniquely identified by the combined selection of the word line to which the gate of the memory cell access device **350***a*-**350***h* is connected, and the cell select line to which the memory cell is connected.

Each word line **330***a*-**330***d* is connected to a word line driver in the form of a row decoder **460** for selecting the respective word line for an access operation. Similarly, each cell select line **320***a*-**320***d* is coupled to a driver in the form of a column decoder **450**.

For simplicity, FIG. **2**B illustrates a memory array having only four rows of memory bit structures **315** on four cell select lines **320***a*-**320***d* and four columns of memory bit structures **315** on four word lines **330***a*-**330***d*. However, it should be understood that in practical applications, the memory device **400** has significantly more memory bit structures in an array. For example, an actual memory device may include several million memory bit structures **315** arranged in a number of subarrays.

Significantly, FIGS. **2**A and **2**B illustrate how each memory cell **10** is connected to a separate and individual access device **350**. As was described above, in resistive memory cells such as the phase change memory cells **10**, the amount of current necessary to change at least a portion of the phase change material **16** into an amorphous state is relatively high (generally a few hundred microamps). As a result, the access device **350** for each memory cell **10** is correspondingly large. In a conventional phase change memory bit structure with a one-to-one correspondence between memory cells and access devices, the typical memory bit area is 16F2, meaning an area equal to 16 F^2, where F is the fabrication resolution. Because of continued desire to reduce the overall footprint of memory bit structures, there is a need to reduce the footprint of resistive memory bit structures, e.g., phase change memory bit structures.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a typical phase change memory cell.

FIGS. **2**A, **2**B and **2**C are schematic and physical representations of a phase change memory bit structure and a corresponding memory device.

FIG. **3** is a schematic representation of a phase change memory bit structure according to a disclosed embodiment.

FIGS. **4**A, **4**B, **4**C and **4**D are schematic and physical representations of a phase change memory bit structure and a corresponding memory device according to a disclosed embodiment.

FIGS. **5**A, **5**B, **5**C and **5**D are representative diagrams and flowcharts of the formation of a rectifying device in a phase change memory bit structure according to a disclosed embodiment.

FIGS. **6**A, **6**B and **6**C are schematic and physical representations of a phase change memory bit structure and a corresponding memory device according to a disclosed embodiment.

FIGS. **7**A, **7**B and **7**C are schematic and physical representations of a phase change memory bit structure and a corresponding memory device according to a disclosed embodiment.

FIGS. **8**A, **8**B, **8**C and **8**D are schematic and physical representations of a phase change memory bit structure and a corresponding memory device according to a disclosed embodiment.

FIGS. **9**A, **9**B and **9**C are schematic and physical representations of a phase change memory bit structure and a corresponding memory device according to a disclosed embodiment.

FIGS. **10**A, **10**B and **10**C are schematic and physical representations of a phase change memory bit structure and a corresponding memory device according to a disclosed embodiment.

FIGS. **11**A, **11**B, **11**C and **11**D are schematic and physical representations of a phase change memory bit structure and a corresponding memory device according to a disclosed embodiment.

FIG. **12** illustrates a processor system that includes a memory device according to a disclosed embodiment.

FIGS. **13**A, **13**B and **13**C are schematic and physical representations of a phase change memory bit structure and a corresponding memory device according to a disclosed embodiment.

FIGS. **14**A, **14**B and **14**C are schematic and physical representations of a phase change memory bit structure and a corresponding memory device according to a disclosed embodiment.

FIGS. **15**A, **15**B and **15**C are schematic and physical representations of a phase change memory bit structure and a corresponding memory device according to a disclosed embodiment.

DETAILED DESCRIPTION OF THE INVENTION

The large current requirements in variable resistance memory cells result in large access devices. When a variable resistance memory bit structure has a one-to-one pairing of memory cells to access devices, the memory bit structure has a large footprint. An example of the physical structure of a one-to-one memory cell to access device pairing is shown in FIG. **2**C, which relates to portions of memory device **400** (FIG. **2**B). In FIG. **2**C, a cross-sectional view of the physical organization of two conventional memory bit structures **315***c*, **315***e* is depicted. The memory bit structures **315***c*, **315***e* share the same cell select line **320***b* and bit line **340***b*. Each memory bit structure **315***c*, **315***e* in FIG. **2**C includes a memory cell **10***a*, **10***b*, respectively, that each include a top electrode **18**, a bottom electrode **14**, and a phase change region **16** positioned in between the electrodes **14**, **18**. The top electrode **18** of both memory cells **10***a*, **10***b* is connected to the cell select line **320***b*. The bottom electrode **14** of each memory cell **10***a*, **10***b* is connected to the drains of separate and individual access devices **350***c*, **350***e*. The opposing sources of the access devices **350***c*, **350***e* are connected to a shared bit line **340***b*. The access devices **350***c*, **350***e* are gated by separate word lines **330***b*, **330***c*, which form gates of access devices **350***c*, **350***e*.

Generally, the two access devices **350***c*, **350***e* are located in a single active area **552** of the memory device **400**. Other pairs of access devices are located in neighboring active areas **552**. Active areas **552** are regions of device **400** that have been doped so as to allow formation of one or more access devices **350**, such as transistors. Because the current demands of resistive memory cells **10** are relatively high, the size of the access devices **350**, and hence the size of the active areas **552** are correspondingly large.

The large access devices and active areas have the potential to result in large memory bit structure footprints and sparsely populated memory devices, as illustrated in FIG. 2B. An improved resistive memory bit structure with a reduction in the memory bit structure footprint would allow the fabrication of denser resistive memory devices.

Embodiments of the invention are now disclosed which provide different ways of reducing the resistive memory bit structure footprint. One method of reducing the area required by a phase change memory bit structure and yet still utilizing an access device large enough for the phase-changing currents used in a phase change memory cell is to use more than one memory cell per access device. For example, FIG. **3** illustrates a phase change memory bit structure **615** that incorporates two phase change memory cells **10***a*, **10***b*. Memory cells **10***a*, **10***b* are both coupled to an access device **350** such as a transistor. Each memory cell **10***a*, **10***b* is also connected to a separate cell select line **320***a*, **320***b*. As in the typical phase change memory bit structure **315** of FIG. 2A, the access device **350** is gated by a word line **330**. A bit line **340** provides a source to the access device **350** and is connected to the memory cells **10***a*, **10***b* when the access device **350** is activated by the word line **330** and when one of the memory cells **10***a*, **10***b* is selected by the corresponding cell select line **320***a*, **320***b*, respectively.

The memory bit structure **615** also includes two rectifying devices **660***a*, **660***b* such as, for example, diodes. The rectifying devices **660***a*, **660***b* are each serially connected between the corresponding memory cells **10***a*, **10***b* and the access device **350**. The rectifying devices **660***a*, **660***b* prevent parallel leakage current among the memory cells **10***a*, **10***b*. In other words, when memory cell **10***a* is selected by activation of both the cell select line **320***a* and word line **330**, the resultant current that flows through memory cell **10***a* is prevented from flowing through memory cell **10***b* by rectifying device **660***b*. As will be explained below, the rectifying devices **660***a*, **660***b* may be integrated into the drain regions of the access device **350** when access device **350** is a transistor, or may be separate devices.

Multiple memory bit structures **615** may be organized into an array. FIG. **4**A illustrates a memory device **700** in which memory bit structures **615***a*-**6151** are organized as parallel structures (as opposed to the staggered arrangement illustrated in FIG. 2B). As in the memory device depicted in FIG. 2B, device **700** includes word lines **330***a*-**330***d*, each connected to a word line driver in the form of a row decoder **460** for selecting the respective word line for an access operation. Similarly, device **700** includes cell select lines **320***a*-**320***f* which are each coupled to a driver in the form of a column decoder **450**. For each memory bit structure, two cell select lines and one word line are required, since each memory bit structure includes two memory cells. For example, in FIG. **4**A, memory bit structure **615***d* is connected to both cell select lines **320***a* and **320***b* as well as to the word line **330***b*. In order to select memory cell **10***c*, for example, cell select line **320***a* and word line **330***b* must both be activated. The current passing through the selected memory cell **10***c* may then be measured by sense amplifiers (not shown), in the case of a read operation. In the case of a write operation, a stronger programming current is applied to the memory cell. A write operation for memory cell **10***c* is done by selecting memory cell **10***c* through activation of both the cell select line **320***a* and the word line **330***b*. A voltage differential between the cell select line **320***a* and the bit line **340***a* sufficient to generate a current to program the memory cell **10***c* is created. The voltage differential may be created by altering the voltages of either the cell select line **320***a* or the bit line **340***a*, or through some combination. Generally, the bit lines **340***a*-**340***c* are either tied to ground or to a fixed voltage, though they may be individually addressed.

A cross-sectional view of the physical organization of two memory bit structures **615***a*, **615***d* (FIG. **4**A) in device **700** is represented in FIGS. **4**B and **4**C. FIGS. **4**B and **4**C represent two different cross sectional views over a single active area **852**, as illustrated in the top-down view of FIG. **4**D. The cross-sectional views appear similar, however each view includes a different cell select line **320***a* (FIG. **4**B), **320***b* (FIG. **4**C), different memory cells **10***a*, **10***c* (FIG. **4**B), **10***b*, **10***d* (FIG. **4**C), and different rectifying devices **660***a*, **660***c* (FIG. **4**B), **660***b*, **660***d* (FIG. **4**C). A single memory bit structure **615***a*, **615***d* (FIG. **4**A) includes elements of both FIGS. **4**B and **4**C. Memory bit structure **615***a* (FIG. **4**A) includes word line **330***a* for activating access device **350***a*. When access device **350***a* is activated, bit line **340***a* is coupled to both memory cells **10***a* (FIG. **4**B) and **10***b* (FIG. **4**C) via lower metal layer **1**. The top electrode of memory cell **10***a* is connected to cell select line **320***a* (FIG. **4**B). The top electrode of memory cell **10***b*, however, is coupled to cell select line **320***b* (FIG. **4**C). Thus, memory cells **10***a* and **10***b* share the same word line **330***a*, bit line **340***a* and access device **350***a*, but are coupled to different cell select lines **320***a*, **320***b*. Similarly, memory bit structure **615***d* (FIG. **4**A) includes word line **330***b* for activating access device **350***d*. When access device **350***d* is activated, bit line **340***a* is coupled to both memory cells **10***c* (FIG. **4**B) and **10***d* (FIG. **4**C) via lower metal layer **1**. Memory cell **10***d* is coupled to cell select line **320***b* (FIG. **4**C) and memory cell **10***c* is coupled to cell select line **320***a* (FIG. **4**B).

Each memory cell **10***a*-**10***d* is coupled to an access device **350***a*, **350***d* via a respective rectifying device **660***a*-**660***d*. The rectifying devices **660***a*-**660***d* may be p-n or Schottky diodes formed in the drains of the access devices **350**. Multiple rectifying devices are located within a single access device drain. For example, both memory cells **10***a*, **10***b* are coupled to rectifying devices **660***a*, **660***b* located within the drain of access device **350***a*. The rectifying devices **660***a*, **660***b* may include doped regions that are physically separate from each other, as indicated in FIG. **4**D, or they may share a doped region. In either case, however, the rectifying devices **660***a*, **660***b* function as two separate devices. Similarly, rectifying devices **660***c*, **660***d* are located within the drain of access device **350***d* and may include doped regions that are physically separate from each other or that are shared.

FIG. **4**D is a top-view schematic diagram of active area **852**. FIG. **4**D illustrates the physical relationship of the cross-sectional views of FIGS. **4**B and **4**C to each other. Both cross-sectional views are taken above the same active area **852**. Each cross-sectional view is located over two doped regions that are part of the rectifying devices **660***a*-**660***d*, as explained below in connection with FIGS. **5**A and **5**B. The active area **852** is host to two access devices **350***a*, **350***d*. Access device **350***a* is illustrated as including the upper portion of active area **852** and is bisected by word line **330***a*. Access device **350***d* is illustrated as including the lower portion of active area **852** and is bisected by word line **330***b*. Both access devices **350***a*, **350***d* share bit line **340***a* as a source.

As stated above, the rectifying devices **660***a*-**660***d* may be formed within the drains of the access devices **350***a*, **350***d*. For example, FIG. **5**A illustrates a rectifying device **660** formed as a p-n diode in the drain of access device **350** gated by word line **330**. Method **510** (FIG. **5**B) is used to form the p-n diode illustrated in FIG. **5**A. The components of the access device **350** are formed (step **503**), such as the gate **584** and the source (not shown in FIG. **5**B). The access device drain **582** is also formed and then heavily doped with, for example, arsenic or phosphorous (step **503**). After the access device **350** is formed, inter-level dielectrics (ILD) **586** such as silicon dioxide are deposited in preparation for metal trace deposition and excess deposits are removed via chemical-mechanical polishing (CMP) (step **504**). A via **588** is then etched through the deposited dielectrics **586**, extending to the access device drain **582** (step **506**). Boron implantation is used to dope the bottom of the via **588** to p-type (step **520**). An annealing process is used to cause the p-type doping to diffuse sideways so as to cover the entire bottom of the via **588** (step **520**). The via **588** is then filled with a thin deposited layer of titanium **590** followed by a thin deposited layer of titanium nitride **591** and then tungsten **592** (step **522**). An annealing process is again used, this time to form titanium silicide ($TiSi_2$) **593** from the initially deposited layer of titanium **590** at the bottom of the via **588**, thus reducing the contact resistance (step **524**). Finally, tungsten chemical-mechanical polishing is used to form the tungsten contacts **594** (step **524**).

The rectifying devices **660** may also be Schottky diodes, as illustrated in FIG. **5**C and method **512** of FIG. **5**D. A Schottky diode formation method is similar to the p-n diode formation. In order to form a Schottky diode within the drain **582** of an access device **350**, the portions of the access device **350** are formed and the access device drain **582** heavily doped with, for example, arsenic or phosphorous (step **503**). After the access device **350** is formed, inter-level dielectrics (ILD) **586** such as silicon dioxide are deposited in preparation for metal trace deposition and excess deposits are removed via chemical-mechanical polishing (CMP) (step **504**). A via **588** is then etched through the deposited dielectrics **586**, extending to the access device drain **582** (step **506**). Boron implantation is used to antidope the bottom of the via **588** to n-type (step **530**). An annealing process is used to cause the n-type doping to diffuse sideways so as to cover the entire bottom of the via **588** (step **530**). The via **588** is then filled with deposited platinum **595** (step **532**). An annealing process is again used, this time to foam platinum silicide (PtSi) **596** at the bottom of the via **588** to form the Schottky diode (step **532**). Finally, a dry etch back process or chemical-mechanical polishing is used to form the platinum contacts **597** (step **508**).

As explained above, memory device **700** is one method of implementing memory bit structure **615** (FIG. **3**) into a memory array. However, more efficient designs that conserve memory bit area may be used. For example, FIG. **6**A illustrates an additional method of organizing the memory bit structures **615***a*-**615***f* into an array. In the memory device **800**, memory cells from different memory bit structures are arranged back-to-back with cell select lines **320***a*-**320***d* intersecting the back-to-back memory cells. Physically, the back-to-back memory cells represent two stacked memory cells, with the top memory cell being arranged upside down, as is illustrated in FIG. **6**B, described below. One example of back-to-back stacked memory cells are memory cells **10***a*, **10***e*. As in the memory devices described above, device **800** includes word lines **330***a*-**330***d* and cell select lines **320***a*-**320***d*. For each memory bit structure **615***a*-**615***f*, two cell select lines and one word line are required, since each memory bit structure **615***a*-**615***f* includes two memory cells. For example, in FIG. **6**A, memory bit structure **615***a* is connected to both cell select lines **320***a* and **320***b* as well as the word line **330***b*. In order to select the memory cell **10***a*, cell select line **320***a* and word line **330***b* must both be activated. The current passing through the selected memory cell **10***a* is then measured by sense amplifiers (not shown), in the case of a read operation. In the case of a write operation, a stronger programming current is applied to the memory cell. A write operation for memory cell **10***a* is done by selecting memory cell **10***a* through activation of both the cell select line **320***a* and the word line **330***b*. A voltage differential between the cell select line **320***a* and the bit line **340***b* sufficient to generate a current to program the memory cell **10***a* is created. The voltage differential may be created by altering the voltages of either the cell select line **320***a* or the bit line **340***b*, or through some combination. The bit lines **340***a*-**340***d* may be tied to ground or to a fixed voltage, or may be individually addressed.

In FIG. **6**B, a cross-sectional view of the physical organization of two memory bit structures **615***a*, **615***d* (FIG. **6**A) in device **800** is represented, in addition to partial depictions of other memory bit structures. The portion of FIG. **6**B represented by dashed lines is not in the same cross-sectional plane as the portions of FIG. **6**B represented by solid lines, as also depicted in FIG. **6**C. Memory bit structure **615***a* (FIG. **6**A) includes word line **330***b* for activating access device **350***a*. When access device **350***a* is activated, bit line **340***b* is coupled to both memory cells **10***a*, **10***b* via upper metal **2** and lower metal **1**, respectively. Memory cell **10***a* is an upside-down memory cell stacked on top of a memory cell **10***e* from another memory bit structure. The two memory cells share the same top electrode **18***a*, which is also shared by two additional stacked memory cells. Cell select line **320***a* connects with memory cell **10***a* via the shared top electrode **18***a*. Memory cell **10***b* is the lower of two stacked memory cells **10***f*, **10***b* and is coupled to cell select line **320***b* via a top electrode **18***b*. Similarly, memory bit structure **615***d* (FIG. **6**A) includes word line **330***c* for activating access device **350***d*. When access device **350***d* is activated, bit line **340***b* is coupled to both memory cells **10***c*, **10***d* via lower metal **1** and upper metal **2**, respectively. Memory cell **10***d* is an upside-down memory cell stacked on top of a memory cell **10***h* from another memory bit structure, the two memory cells **10***d*, **10***h* sharing a top electrode **18***c*. Cell select line **320***a* connects with memory cell **10***d* via the shared top electrode **18***c*. Memory cell **10***c* is the lower of two stacked memory cells **10***g*, **10***c* and is coupled to cell select line **320***b* via its top electrode **18***b*.

In the arrangement of memory bit structures **615** in FIGS. **6**A and **6**B, each memory cell **10***a*-**10***d* shares a top electrode **18***a*-**18***c* and connecting cell select line **320***a*, **320***b* with three other memory cells. As a specific example, memory cells **10***b*, **10***c*, **10***f*, **10***g* share top electrode **18***b* and are all connected to cell select line **320***b*. However, each of the four memory cells are activated by a different word line (e.g., 330*a*-330*d*). Each access device **350***a*, **350***d* operates to allow current flow through two different memory cells **10***a*-**10***d* located above different active areas **852***a*-**852***c*. For example, access device **350***a* controls access to memory cell **10***a* located above active area **852***a* and memory cell **10***b* located above active area **852***b*. In this way, the overall memory bit area is reduced through both a single access transistor servicing two memory cells as well as the stacking of memory cells on top of each other.

Each memory bit structure **615***a*, **615***d* also has rectifying devices **660***a*-**660***d* which, in this embodiment, have been formed within the drain of the access devices **350***a*, **350***d*. As in device **700** of FIGS. **4**A-**4**D, the rectifying devices **660***a*-**660***d* may be formed using, for example, p-n diodes or Schottky diodes, as explained in relation to FIGS. **5**A and **5**B.

FIG. **6**C represents a top-down view of a portion of memory device **800**. In FIG. **6**C, each active area **852***a*-**852***c* includes two access devices. For example, access devices **350***a* and **350***d* are in the active area **852***b*. Within active area **852***b*, access device **350***a* is gated by word line **330***b* and, when activated, couples bit line **340***b* to memory cells **10***a* (FIG. **6**B), located above active area **852***a* and memory cell **10***b* (FIG. **6**B), located above active area **852***b*. Similarly, access device **350***d* is gated by word line **330***c* and, when activated, couples bit line **340***b* to memory cells **10***c*, **10***d*, located above active areas **852***b*, **852***c*, respectively. In each case, the controlling access device **350***a*, **350***d* controls access to memory cells that are located above two adjacent but staggered active areas (e.g., **852***a*, **852***c*). Memory cells that are located above active areas that are adjacent to the active area wherein the controlling access device is located are coupled to their controlling access devices via a metal **2** trace and a rectifying device **660***a*-**660***d*. The rectifying device **660***a*-**660***d* is formed within the drain of the controlling access device **350***a*, **350***d* and is represented in FIG. **6**C as a doped region **660***a*-**660***d*.

An additional method of organizing the memory bit structures **615** into an array is illustrated in FIG. **7**A. In FIG. **7**A, memory device **900** includes memory cells from different memory bit structures **615***a*-**615***d* that are arranged back-to-back with cell select lines **320***a*-**320***c* intersecting the back-to-back memory cells. The primary difference between the organization of memory device **800** and memory device **900** is that the memory bit structures **615***a*-**615***d* in device **900** are arranged in a parallel manner and are not staggered as in device **800**. The parallel structure results in a tighter access device **350***a*-**350***d* layout. In order to achieve the parallel layout, the two memory cells in each memory bit structure are arranged above diagonally proximate active areas **852***a*-**852***d*, as illustrated in FIG. **7**C.

FIG. **7**B represents a cross-sectional view of the physical organization of two memory bit structures **615***a*, **615***c* in device **900**. The portion of FIG. **7**B represented by dashed lines is not in the same cross-sectional plane as the portions of FIG. **7**B represented by solid lines. Memory bit structure **615***a* (FIG. **7**A) includes word line **330***c* for activating access device **350***a*. When access device **350***a* is activated, bit line **340***b* is coupled to both memory cells **10***a*, **10***b* via upper metal **2** and lower metal **1**, respectively. Memory cell **10***a* is an upside-down memory cell stacked on top of a memory cell **10***e* from another memory bit structure. The two memory cells **10***a*, **10***e* share the same top electrode **18***a*, which is also shared by two additional stacked memory cells **10***c*, **10***g*. Cell select line **320***a* connects with memory cell **10***a* via the shared top electrode **18***a*. Memory cell **10***b* is the lower of two stacked memory cells **10***f*, **10***b* and is coupled to cell select line **320***b* via a top electrode **18***b*. Similarly, memory bit structure **615***c* (FIG. **7**A) includes word line **330***d* for activating access device **350***c*. When access device **350***c* is activated, bit line **340***b* is coupled to both memory cells **10***c*, **10***d* via lower metal **1** and upper metal **2**, respectively. Memory cell **10***c* is an upside-down memory cell stacked on top of a memory cell **10***g* from another memory bit structure, the two memory cells **10***c*, **10***g* sharing a top electrode **18***a*. Cell select line **320***a* connects with memory cell **10***d* via the shared top electrode **18***a*. Memory cell **10***d* is the lower of two stacked memory cells **10***h*, **10***d* and is coupled to cell select line **320***b* via its top electrode **18***b*. Bit lines **340***a*-**340***c* are individually addressed.

The arrangement of the memory bit structures **615***a*-**615***d* in device **900** differs from the physical arrangement of the memory bit structures in device **800** in that the two memory bit structures **615***a*, **615***c* depicted in FIG. **7**B are located above only two active areas, **852***a*, **852***d*. In device **800**, three active areas are used to implement any pair of memory bit structures. The reduced number of active areas used by the memory bit structures **615***a*-**615***d* in device **900** allows the active areas **852***a*-**852***d* to be arranged in a parallel orientation (as opposed to a staggered orientation as depicted in FIG. **6**C).

In the top-down view of FIG. **7**C, each active area **852***a*-**852***d* includes two access devices. The access devices **350***a* and **350***c* that control access to the memory bit structures **615***a* and **615***c* are both located in active area **852***d*. Within active area **852***d*, access device **350***a* is gated by word line **330***c* and, when activated, couples bit line **340***b* to memory cell **10***a* (FIG. **7**B) located above active area **852***a* and memory cell **10***b* (FIG. **7**B) located above active area **852***d*. Similarly, access device **350***c* is gated by word line **330***d* and, when activated, couples bit line **340***b* to memory cells **10***c*, **10***d*, also located above active areas **852***d* and **852***a*, respectively. In both cases, access devices **350***a*, **350***c* control access to memory cells that are located in two different active areas **852***a*, **852***d*.

FIGS. **13**A-**13**C represent a similar circuit (memory device **2300** in FIG. **13**A), organization and arrangement as shown in FIGS. **7**A-**7**C. However, in FIGS. **13**A-**13**C, more than one memory cell shares the same cell select line and word line. For example, in FIG. **13**A, memory bit structures **615***a* and **615***b* include memory cells **10***b*, **10***c*, respectively. Both memory cells **10***b*, **10***c* are activated by utilizing cell select line **320***b* and word line **330***a*. As a result, memory cell selection requires that the bit lines **340***b*, **340***c* be individually addressed. For example, memory cell **10***b* is selected by activating the word line **330***a* and the cell select line **320***b*, and by appropriately biasing the bit line **340***b*. Similarly, memory cell **10***c* is selected by activating word line **330***a* and cell select line **320***b*, and by appropriately biasing the bit line **340***c*.

Another improved memory bit structure that results in reduced memory bit area is illustrated in FIG. **8**A. FIG. **8**A represents a memory bit structure **1015** that is similar to the memory bit structure **615** of FIG. **3** except that the rectifying devices **660***a*, **660***b* have been moved so as to be positioned in between the memory cells **10***a*, **10***b* and the cell select lines **320***a*, **320***b*. The rectifying devices **660***a*, **660***b* are preferably silicon p-n diodes or Schottky diodes but are, in this embodiment, not formed within the drains of an access device **350**. In the memory bit structure **1015**, one rectifying device can service two memory cells, each of which is from a different memory bit structure **1015**. Thus, the reduction in components results in an overall reduction in memory bit area.

FIG. 8B illustrates a memory device 1000 that includes a staggered arrangement of the memory bit structures 1015a-1015f. As in the memory devices 800, 900, the memory cells in memory device 1000 are stacked. This time, however, the cell select lines 320a-320d connect first to a rectifying device (e.g., 660a-660d) and then to the top electrodes of the stacked memory cells 10a-10h.

FIG. 8C illustrates a cross-sectional view of the physical organization of two memory bit structures 1015b, 1015d in device 1000, in addition to partial depictions of other memory bit structures. The dashed lines in FIG. 8C represent structures that are not in the same viewing plane as those depicted using solid lines. However, by referencing the top-down view of FIG. 8D, it is apparent that some "solid" structures are in different planes than other depicted "solid" structures. A similar statement may be made regarding the "dashed line" structures. In other words, the structures depicted in FIG. 8C are located within multiple viewing planes; hence FIG. 8C should be viewed in conjunction with FIG. 8D.

One of the significant differences between the cross-sectional view of memory device 1000 shown in FIG. 8C and the cross-sectional view of memory device 800 in FIG. 6B is the absence of the rectifying devices 660a-660d in the access device drains and the presence of rectifying devices 660a-660d connected to the cell select lines 320a, 320b. The rectifying devices 660a-660d are formed by the junction of material layers 661, 662. Material layer 661 is formed within the vias connecting the cell select lines 320a, 320b to the memory cells 10a-10h. Material layer 662 is formed as a layer directly underneath the cell select lines 320a, 320b. The junction between material layers 661 and 662 is a junction between two oppositely doped regions. Material layers 661, 662 may be formed of various materials such as doped polysilicon and titanium or platinum, as long as the junction of the two layers forms a rectifying device 660a-660d such as a p-n diode or a Schottky diode.

Similar to that explained above in conjunction with FIG. 6B, memory bit structure 1015b (FIG. 8B) includes word line 330b for activating access device 350b. When access device 350b is activated, bit line 340b is coupled to both memory cells 10a, 10b. Memory cell 10a is an upside-down memory cell stacked on top of a memory cell 10e from another memory bit structure. Cell select line 320a connects with memory cell 10a via rectifying device 660a. Memory cell 10b is the lower of two stacked memory cells 10f, 10b and is coupled to cell select line 320b via rectifying device 660b. Similarly, memory bit structure 1015d (FIG. 8B) includes word line 330c for activating access device 350d. When access device 350d is activated, bit line 340b is coupled to both memory cells 10c, 10d. Memory cell 10d is an upside-down memory cell stacked on top of a memory cell 10h from another memory bit structure. Cell select line 320a connects with memory cell 10d via rectifying device 660d. Memory cell 10c is the lower of two stacked memory cells 10g, 10c and is coupled to cell select line 320b via rectifying device 660c.

FIG. 8D represents a top-down view of the memory bit structures 1015b and 1015d depicted in FIG. 8C. As in devices 700, 800 and 900, each active area 1052a-1052c includes two access devices. However, active areas 1052a-1052c are different from the active areas used in devices 700, 800 and 900 in that active areas 1052a-1052c do not include one or more rectifying devices. In FIG. 8D, access devices 350b and 350d are in the active area 1052b. Within active area 1052b, access device 350b is gated by word line 330b and, when activated, couples bit line 340b to memory cell 10a (FIG. 8C) located above active area 1052a and memory cell 10b (FIG. 8C) located above active area 1052b. Similarly, access device 350d is gated by word line 330c and, when activated, couples bit line 340b to memory cell 10c (FIG. 8C) located above active area 1052b and memory cell 10d (FIG. 8C) located above active area 1052c. Note that access devices 350b, 350d control access to memory cells that are located in two adjacent but staggered active areas 1052a, 1052c.

Similar to memory devices 900 and 2300, the bit lines 340a-340d in device 1000 must be appropriately biased in order to select a memory cell. In other words, selection of a memory cell requires selecting the corresponding word line, cell select line and bit line. Also, the rectifying devices 660b and 660c may also be merged into one rectifying device connecting a common top electrode similar to memory device 900.

A modification to device 1000 is depicted in FIG. 9A. In FIG. 9A, memory device 1100 includes a parallel arrangement of memory bit structures 1015a-1015i. Each memory bit structure 1015a-1015i includes a single access device 350a-350i and two memory cells (e.g., 10a-10d). The memory cells are stacked with memory cells from adjacent memory bit structures, as depicted in FIG. 9B. For example, memory cells 10a, 10e are stacked; memory cells 10c, 10g are also stacked. A rectifying device (e.g., 660a-660c) is connected between each memory cell and the cell's corresponding cell select line 320a-320d. Significantly, in device 1100, only one rectifying device is used for up to four memory cells. Each of the four memory cells connected to the same rectifying device is from a different memory bit structure. The rectifying devices 660a-660c, as described in relation to FIG. 8C, are formed from the junctions of material layers 661 and 662, wherein the junction represents a boundary between two oppositely doped regions. For example, the top portion of material layer 661 could be n-doped, and the portion of material layer 662 near the junction could p-doped, thus forming a p-n diode. As described above, a Schottky diode may also be formed.

FIG. 9B illustrates a cross-sectional view of the physical organization of two memory bit structures 1015a, 1015d in device 1100, in addition to partial depictions of other memory bit structures. The dashed lines in FIG. 9B represent structures that are not in the same viewing plane as those depicted using solid lines. Also, the structure indicated over active area 1052b in FIG. 9B has been shifted for viewing purposes, but is in reality located behind the structure located over active area 1052a (refer to FIG. 9C for further clarity).

In FIG. 9B, cell select lines 320a, 320b are connected to the memory cell top electrodes 18a-18c via rectifying devices 660a-660c. Each rectifying device 660a-660c couples a cell select line 320a, 320b to four memory cells. For example, the structure above active area 1052a depicts cell select line 320a coupled to memory cells 10a, 10e, 10c, 10g via rectifying device 660a. In this way, the number of physical components or structures per each memory bit structure is reduced, and the overall structure of device 1100 is simplified. The reduction in structures also allows the memory bit structures 1015a-1015i (FIG. 9A) to be fabricated more compactly.

In FIG. 9B, memory bit structures 1015a and 1015d are depicted. In memory bit structure 1015a, word line 330b may be used to activate access device 350a. When access device 350a is activated, bit line 340b is coupled to both memory cells 10a, 10b. Memory cell 10a is an upside-down memory cell stacked on top of a memory cell 10e from another memory bit structure. Cell select line **320***a* connects with memory cell **10***a* via rectifying device **660***a*. Memory cell **10***b* is the lower of two stacked memory cells **10***f*, **10***b* and is coupled to cell select line **320***b* via rectifying device **660***b*. Similarly, memory bit structure **1015***d* (FIG. **9**A) includes word line **330***c* for activating access device **350***d*. When access device **350***d* is activated, bit line **340***b* is coupled to both memory cells **10***c*, **10***d*. Memory cell **10***c* is an upside-down memory cell stacked on top of a memory cell **10***g* from another memory bit structure. Cell select line **320***a* connects with memory cell **10***c* via rectifying device **660***a*. Memory cell **10***d* is the lower of two stacked memory cells **10***h*, **10***d* and is coupled to cell select line **320***b* via rectifying device **660***c*.

FIG. **9**C represents a top-down view of the memory bit structures **1015***a*, **1015***d* depicted in FIG. **9**B. Each active area **1052***a*-**1052***d* includes two access devices. In FIG. **9**C, access device **350***a* is in the active area **1052***b*. Access device **350***d* is in the active area **1052***d*. Within active area **1052***b*, access device **350***a* is gated by word line **330***b* and, when activated, couples bit line **340***b* to memory cell **10***a* (FIG. **9**B) located above active area **1052***a* and memory cell **10***b* (FIG. **9**B) located above active area **1052***b*. Similarly, access device **350***d* is gated by word line **330***c* and, when activated, couples bit line **340***b* to memory cell **10***c* (FIG. **9**B) located above active area **1052***a* and memory cell **10***d* (FIG. **9**B) located above active area **1052***d*. The parallel configuration of the active areas **1052***a*-**1052***d* results in device **1100** being more dense and area efficient than devices where the active areas are staggered.

FIGS. **14**A-**14**C represent a similar circuit (memory device **2400** in FIG. **14**A), organization and arrangement as shown in FIGS. **9**A-**9**C. However, in FIGS. **14**A-**14**C, more than one memory cell shares the same cell select line and word line. For example, in FIG. **14**A, memory bit structures **1015***a* and **1015***b* include memory cells **10***c*, **10***d*, respectively (among others). Both memory cells **10***c*, **10***d* are activated by utilizing cell select line **320***b* and word line **330***a*. As a result, memory cell selection requires that the bit lines **340***b*, **340***c* be individually addressed. For example, memory cell **10***c* is selected by activating the word line **330***a* and the cell select line **320***b*, and by appropriately biasing the bit line **340***b*. Similarly, memory cell **10***d* is selected by activating word line **330***a* and cell select line **320***b*, and by appropriately biasing the bit line **340***c*.

FIG. **10**A depicts a memory device **1200** that includes a parallel arrangement of memory bit structures **1015***a*-**1015***f*, organized in a way that only two memory cells are coupled to a rectifying device. Device **1200** makes this possible by spacing the two memory cells controlled by the same access device at least two access devices apart, as illustrated in FIGS. **10**A and **10**C. FIG. **10**B depicts a cross-sectional view of the physical structure of two memory bit structures **1015***a*, **1015***d* from device **1200**. FIG. **10**C depicts the top-down view of the structures in FIG. **10**B. In each of these figures, a memory cell **10***a*-**10***d* shares a rectifying device **660***a*-**660***d* with one other memory cell. For example, memory cell **10***a* shares rectifying device **660***a* with another memory cell **10***e* upon which memory cell **10***a* is stacked. Memory cell **10***c* also shares access device **350***d* with memory cell **10***d*. Long metal interconnects (metal **1** and **2**) connect remote memory cells **10***a* and **10***c* to the access devices **350***a* and **350***d*, respectively. The metal interconnects (metal **1** and **2**) make it possible to distribute portions of the memory bit structure **1015***a*, **1015***d* to distant active areas (e.g., **1052***a*). Effectively, the device **1200** combines the benefits of a staggered active area layout with the compactness of a parallel active area layout. In device **1200**, individual bit lines **340***a*-**340***d* may be individually addressed accordingly to the cell to be selected.

FIG. **15**A represents a memory device **2500** that is similar to memory device **1200** of FIG. **10**A. FIGS. **15**B and **15**C represent the corresponding organization and arrangement of memory device **2500**. In memory device **2500**, more than one memory cell shares the same cell select line and word line. For example, in FIG. **15**A, memory bit structures **1015***a* and **1015***b* include memory cells **10***b*, **10***c*, respectively (among others). Both memory cells **10***b*, **10***c* are activated by utilizing cell select line **320***b* and word line **330***a*. As a result, memory cell selection requires that the bit lines **340***b*, **340***c* be individually addressed. For example, memory cell **10***b* is selected by activating the word line **330***a* and the cell select line **320***b*, and by appropriately biasing the bit line **340***b*. Similarly, memory cell **10***c* is selected by activating word line **330***a* and cell select line **320***b*, and by appropriately biasing the bit line **340***c*.

The general concepts discussed above can be applied to more complex memory bit structures. For example, in FIG. **11**A, the concepts of memory bit structures **615** (FIG. **3**) and **1015** (FIG. **8**A) are extended to a one access device/three memory cell memory bit structure **1315**. In structure **1315**, the rectifying devices **660***a*-**660***c* are connected in between the memory cells **10***a*-**10***c* and their respective cell select lines **320***a*-**320***c*. In this way, a single access device **350** may control three memory cells **10***a*-**10***c*. In fact, a single access device **350** could control access to as many memory cells as desired using the same basic layout shown in FIG. **11**A. The memory bit structure **1315** may be arranged in a memory device **1300**, as represented in FIG. **11**B. In FIG. **11**B, a cell select line **320***a*-**320***i* exists for each memory cell in the memory bit structure **1315***a*-**1315***l*. Although each memory bit structure **1315***a*-**1315***l* in device **1300** only depicts three memory cells, as many memory cells as desired may be added with corresponding cell select lines.

FIG. **11**C depicts one possible method of physically arranging the memory bit structures **1315***a*, **1315***d*. For example, in FIG. **11**C, word line **330***a* is used to activate access device **350***a*, thereby coupling bit line **340***a* to the bottom electrodes of memory cells **10***a* through **10***x*, where 'x' represents any letter of the alphabet. Each memory cell's top electrode is also coupled to a cell select line (e.g., **320***a*-**320***x*) via a rectifying device (e.g., **660***a*-**660***x*). Memory cell **10***a* is connected to cell select line **320***a*. Memory cell **10***x* is connected to cell select line **320***x*. The memory bit structures **1315***a*, **1315***d* illustrated in FIG. **11**C are also shown in a top-down view in FIG. **11**D. In FIG. **11**D, it is apparent that a pair of the memory bit structures (e.g., **1315***a*, **1315***d*) are staggered onto a single active area **1052**. In this way, as many memory cells as desired may be located above a single active area **1052** and access device **350***a*, **350***d*.

Each of the improved phase change memory devices **700**-**1300** improves the spatial efficiency of phase change memory bit structures by utilizing only one access device for multiple memory cells. Spatial efficiency is also improved by stacking memory cells on top of each other and by sharing rectifying devices between memory cells. A parallel arrangement of memory bit structures also results in improved spatial efficiency.

It should be appreciated that the improved phase change memory devices **700**-**1300** may be fabricated as part of an integrated circuit. The corresponding integrated circuits may be utilized in a typical processor system. For example, FIG. **12** illustrates a simplified processor system **1500** which includes a memory device **1400** employing improved phase change memory bit structures such as structures **615**, **1015** and **1315** in accordance with the above described embodiments. A processor system, such as a computer system, generally comprises a central processing unit (CPU) **1510**, such as a microprocessor, a digital signal processor, or other programmable digital logic devices, which communicates with an input/output (I/O) device **1520** over a bus **1590**. The memory device **1400** communicates with the CPU **1510** over bus **1590** typically through a memory controller.

In the case of a computer system, the processor system **1500** may include peripheral devices such as removable media devices **1550** (e.g., CD-ROM drive or DVD drive) which communicate with CPU **1510** over the bus **1590**. Memory device **1400** is preferably constructed as an integrated circuit, which includes one or more phase change memory devices. If desired, the memory device **1400** may be combined with the processor, for example CPU **1510**, as a single integrated circuit.

It should also be appreciated that various embodiments have been described as using a phase change material as an exemplary resistance variable material. The invention may also be used in other types of resistive memory to improve current flow through whatever resistance variable material is used.

The above description and drawings should only be considered illustrative of exemplary embodiments that achieve the features and advantages described herein. Modification and substitutions to specific process conditions and structures can be made. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A resistive memory structure, comprising:

at least one pair of stacked resistive memory cells;

a plurality of access devices, each access device being coupled to a respective one of the stacked resistive memory cells; and

a common electrode being positioned between the memory cells in each of the at least one pair of stacked resistive memory cells and coupling each stacked resistive memory cell to a cell select line via a rectifying device.

2. The resistive memory structure of claim **1**, wherein the rectifying device is formed at least partially within the cell select line.

3. The resistive memory structure of claim **1**, further comprising two pairs of stacked resistive memory cells.

4. The resistive memory structure of claim **3**, wherein the two pairs of stacked resistive memory cells share the common electrode that is positioned between the memory cells in each of the two pairs of stacked resistive memory cells.

5. The resistive memory structure of claim **4**, wherein each of the two pairs of stacked resistive memory cells includes an upper memory cell and a lower memory cell, the lower memory cells being closer to a plane that includes the access devices than the upper memory cells.

6. The resistive memory structure of claim **5**, wherein the access devices coupled to the lower memory cells are positioned in an active area aligned with a position of the two pairs of stacked resistive memory cells.

7. The resistive memory structure of claim **5**, wherein the access devices coupled to the upper memory cells are positioned in active areas that are offset from the position of the two pairs of stacked resistive memory cells.

8. The resistive memory structure of claim **7**, wherein the offset active areas are offset in a parallel arrangement with respect to the aligned active area.

9. The resistive memory structure of claim **7**, wherein the offset active areas are offset in a checkerboard with respect to the aligned active area.

10. A phase change memory device, comprising:

an array of access devices;

an array of pairs of stacked phase change memory cells, each pair including an upper and a lower phase change memory cell, the lower phase change memory cell being coupled to an access device that is horizontally aligned with the respective stacked pair of memory cells, while the upper phase change memory cell is coupled to an access device that is horizontally offset from the respective stacked pair of memory cells; and

a plurality of rectifying devices, each rectifying device being connected to a memory cell.

11. The device of claim **10**, wherein the rectifying devices are configured between each memory cell and each access device.

12. The device of claim **11**, wherein the plurality of rectifying devices are formed at least partially within the plurality of access devices.

13. The device of claim **10**, wherein the rectifying devices are configured between each memory cell and a plurality of cell select lines.

14. The device of claim **13**, wherein the rectifying devices are formed at least partially within the cell select lines.

15. The device of claim **13**, wherein four memory cells share a single rectifying device.

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